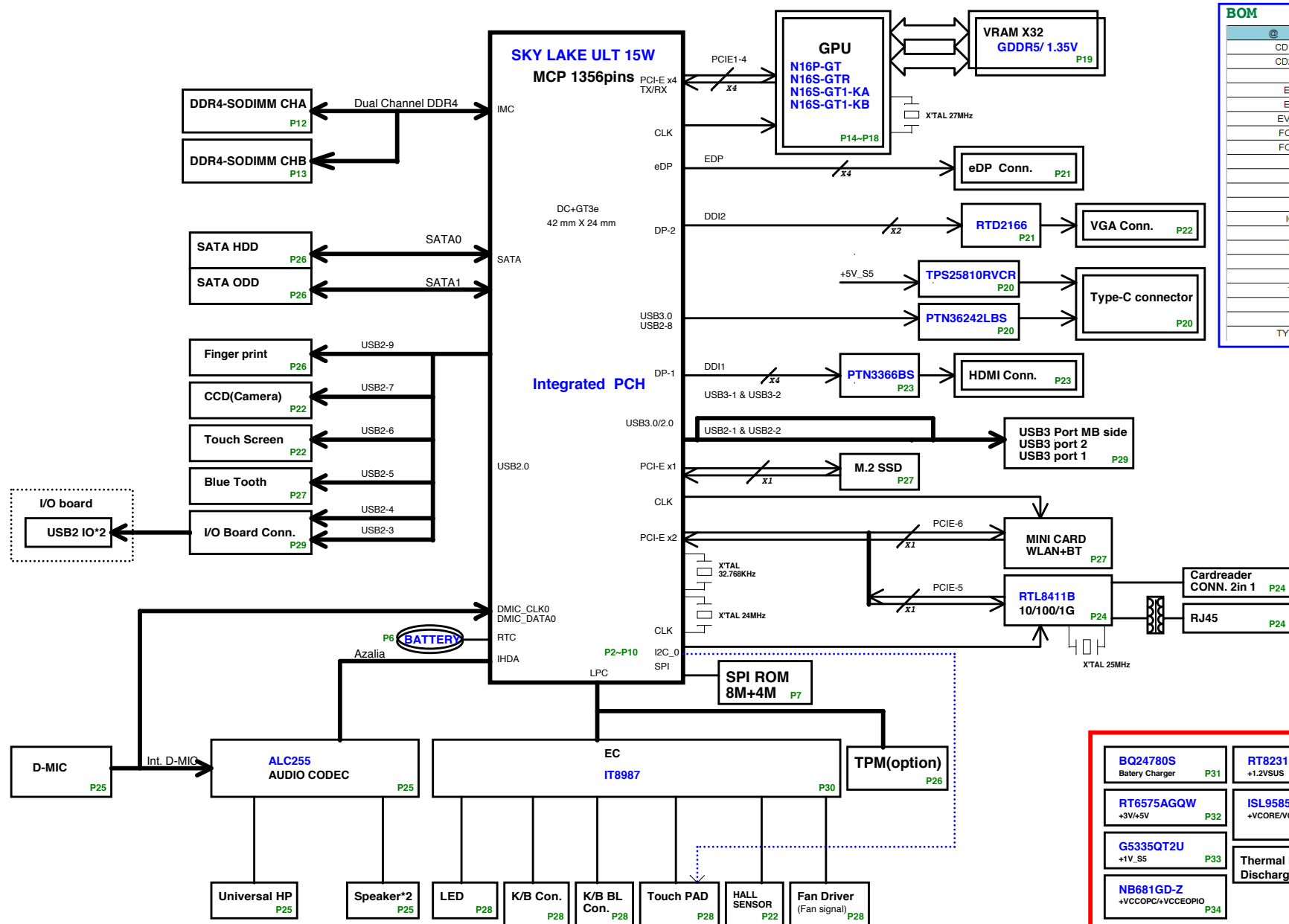


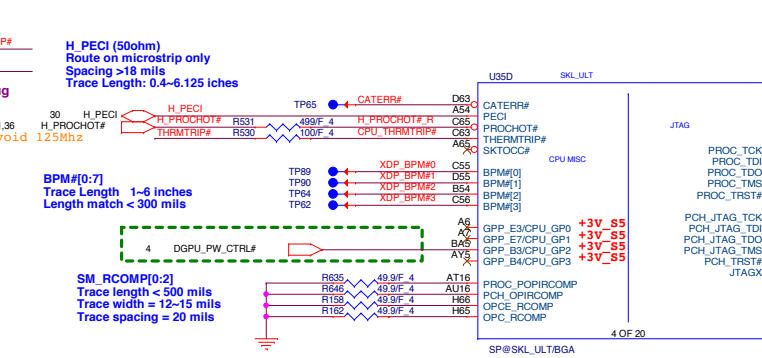
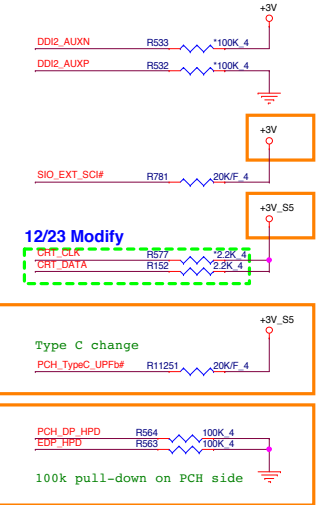
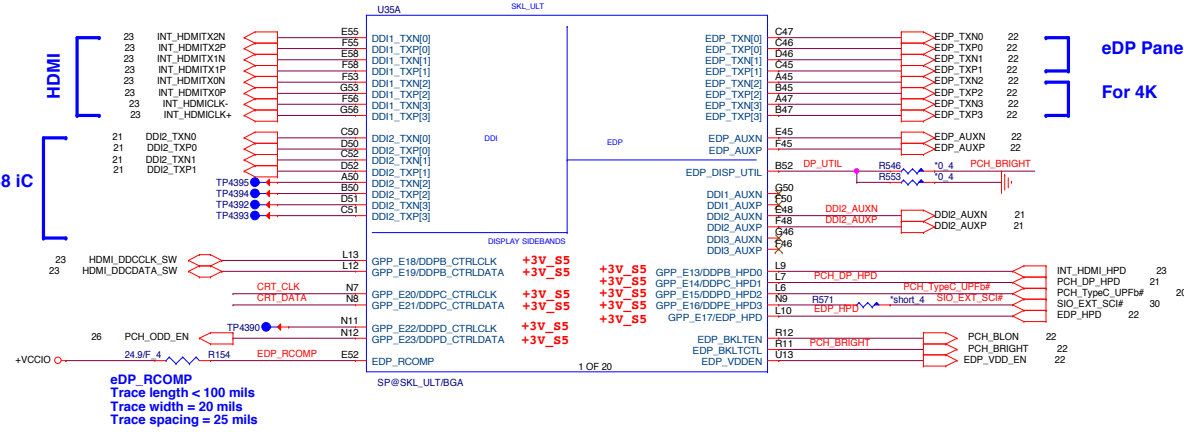
ZAAA Serials SkyLake-U SYSTEM BLOCK DIAGRAM



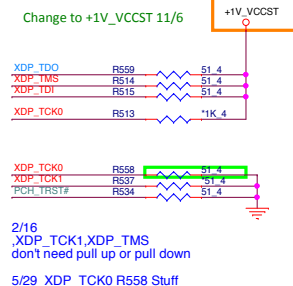
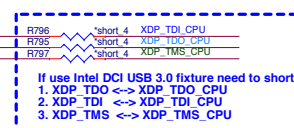
②	Function
CD1006②	22uF_0603 cost down to 10uF_0603
CD2208②	47uF_0805 cost down to 22uF_0805
EV_②	Discrete
EV_A②	Discrete_940M_Kill B channel
EV_B②	Discrete_940M_Kill A channel
EV_SP②	Discrete_Spectral part
FOR15②	For 15"
FOR17②	For 17"
FPD②	Finger Print
GC6②	Discrete_GC6
GS②	G-sensor
GT3②	UMA_GT3
IOAC②	with IOAC
IV②	UMA
NAC②	w/o IOAC
SP②	Spectral Part
TDI②	Touchpad INT
TPM②	TPM
TSU②	Touch Screen USB
TSI②	Touch Screen i2C
TYPEC②	Type-C function

BQ24780S Batery Charger P31	RT8231BGW +1.2VSUS P35	UP1658RQKF +VGPU_CORE P36
RT6575AGWQ +3V/+5V P32	ISL95859HRTZ-T +VCORE/VCCSA/VCCGT P36	RT8068AZWQ +1.05V_GFX P41
G5335QT2U +1V_S5 P33	Thermal Protection Discharger P39	G5335QT2U +1.35V_GFX P41
NB681GD-Z +VCCOPCI+VCCOEPIO P34		

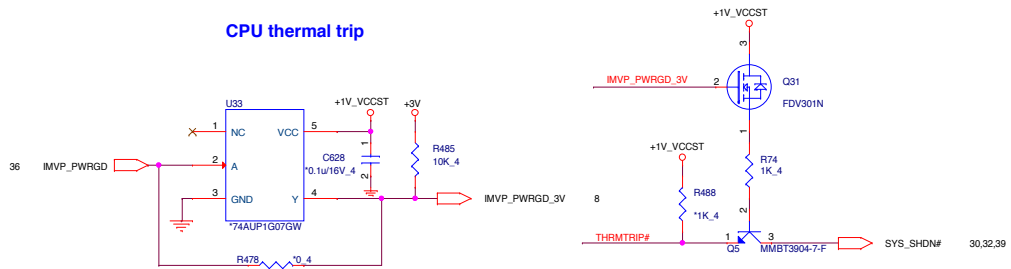
Skylake ULT (DISPLAY,eDP)



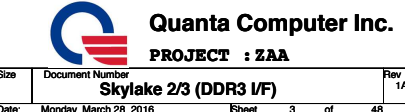
PCH JTAG



CPU thermal trip



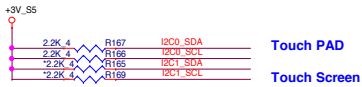
1

SKL ULT (DDR3L)

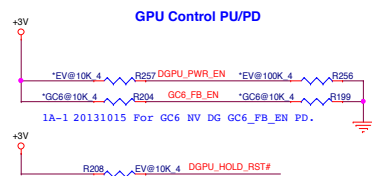
SKL ULT (SIDE BAND) GPIO

H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 inches

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches

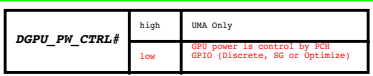


PU 2.2K for touch pad I2C bus(400 KHz)



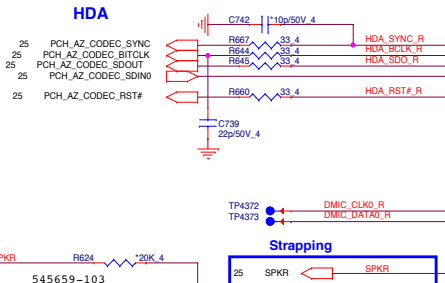
Touch PAD

Touch Screen

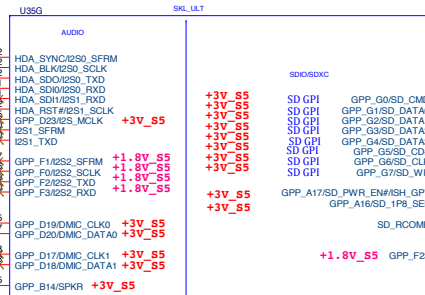


DGPU_PWROK PD on GPU side

	DGPU_PW_CTRL#	VGA H/W Signal	Setup Menu	
UMA Only	1	UMA	Hidden	UMA boot
SG/Optimise	0	GPU	Hidden	GPU boot









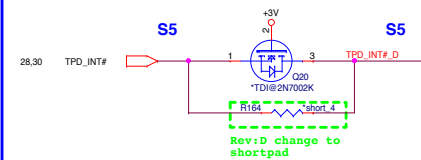
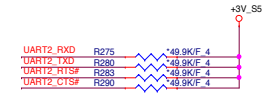
Strapping



SP@SKL_ULT/BGA

Skylake-U Strapping Table

Pin Name	Strap description	Sampled	Configuration	note
GPP_B14 (SPKR)	Top-Block Swap override	PCH_PWROK	0 = "Disable Top Swap (iPD 20K) 1 = Enable Top Swap Mode	+3V  SPKR
GPP_B18 (GSPi0_MOSI)	No reboot	PCH_PWROK	0 = "Disable No Reboot (iPD 20K) 1 = Enable No Reboot Mode	+3V  GSPi0_MOSI
GPP_C2 (SMBALERT#)	TLS Confidentiality	RSMRST#	0 = "Disable Intel ME Crypt to TLS (iPD 20K) 1 = Enable Intel ME Crypt to TLS	+3V_SS  SMBALERT# 7
GPP_B22 (GSPi1_MOSI)	Boot BIOS Strap Bit (BBS)	PCH_PWROK	0 = "SPi (iPD 20K) 1 = LPC	+3V  GSPi1_MOSI
GPP_C5 (SML0ALERT#)	eSPi or LPC	RSMRST#	0 = "LPC is selected for EC (iPD 20K) 1 = eSPi selected for EC	+3V_SS  SML0ALERT# 7
SPI0_MOSI	Reserved	RSMRST#	(iPU 15 ~ 40K)	
SPI0_MISO	Reserved	RSMRST#	(iPU 15 ~ 40K)	
GPP_B23 (SML1ALERT# /PCHHOT#)	Reserved	RSMRST#	(iPD 20K)	
SPI0_IO2	Reserved	RSMRST#	(iPU 15 ~ 40K)	
SPI0_IO3	Reserved	RSMRST#	(iPU 15 ~ 40K)	
HDA_SDO / I2S_TXD0	Flash Descriptor Security Override / Intel ME Debug Mode	PCH_PWROK	0 = "Enable security in the Flash Description (iPD 20K) 1 = Disable Flash Descriptor Security (Override)	change location to near CPU to prevent impact HDA_SDO signal  ME_WR# 30
GPP_E19 (DDPB_CTRLDATA)	Display Port B Detected	PCH_PWROK	0 = "Port B is not detected (iPD 20K) 1 =Port B is detected	
GPP_E21 (DDPC_CTRLDATA)	Display Port C Detected	PCH_PWROK	0 = "Port C is not detected (iPD 20K) 1 =Port C is detected	



Skylake ULT (GPU, SATA , ODD, CLK ,USB2&3)

+3V	2,4,7,8,9,12,13,14,16,21,22,23,24,25,26,27,28,30,32,33,34,35,36,39,40,41
+3V_S5	2,3,4,7,8,9,11,20,24,26,27,28,30,32,34,35,40
+3VPCU	9,11,22,24,25,26,27,28,30,31,32,39,40,41
+3V_RTC	8,9,30
+1V_S5	9,33

dGPU PEG#4

For Thunderbolt

HDD

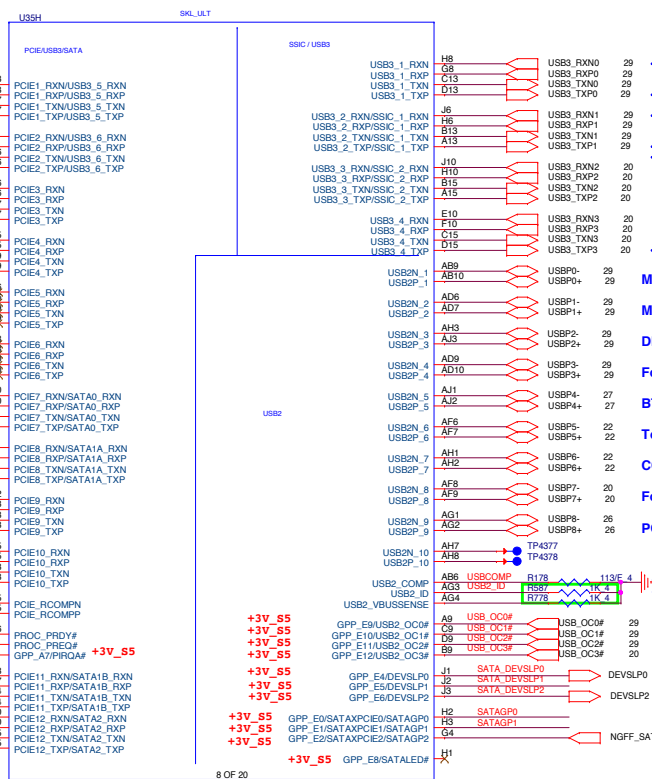
ODD

LAN

WIFI

For M.2 SSD -NA

For M.2 SSD -1



MB USB3.0 (Charger IC)

MB USB3.0

For TYPE-C

MB USB3.0 (Charger IC)

MB USB3.0

DB USB2.0

For 17" DB use

BT

Touch Screen

CCD

For TYPE-C

POA

USBCOMP

Impedance = 50 ohm

Trace length < 500 mils

Trace spacing = 15 mils

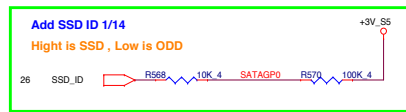
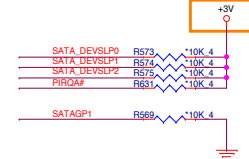
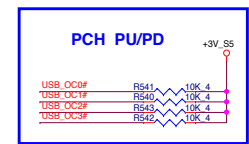
MB U3

MB U3

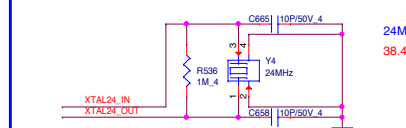
MB U3

MB U3

MB U3



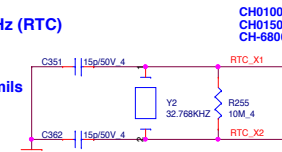
Skylake-U used 24 MHz (50 Ohm ESR) XTAL



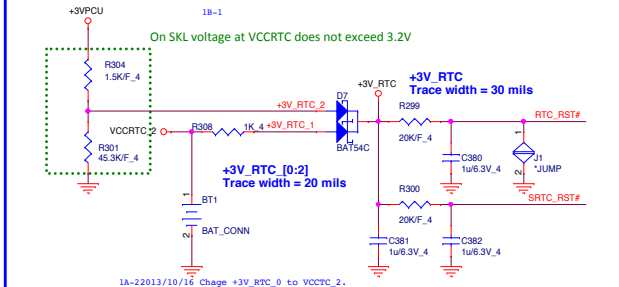
Note: Change Y4 to 38.4 MHz(ESR 30 ohm) for Cannonlake U

RTC Clock 32.768KHz (RTC)

Trace length < 1000 mils



RTC Circuitry (RTC)



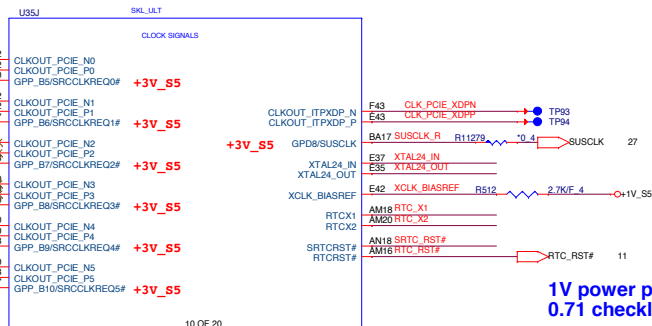
1. AHL03003057 DBV CR2032
2. AHL03003003 VDE CR2032

M.2 SSD

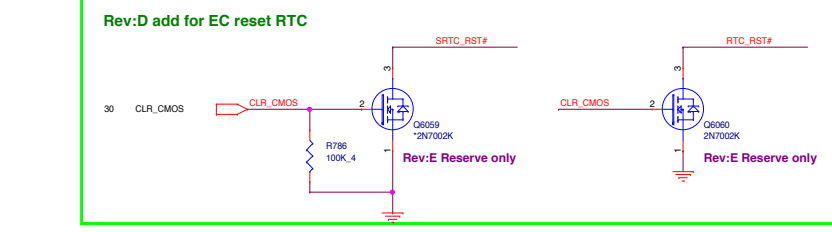
For Thunderbolt

LAN

WLAN



1V power plane
0.71 checklist p14



For M.2 wifi module must

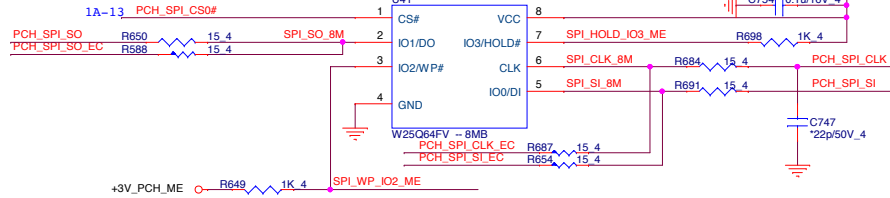
SP@ socket P/N: DFHS08FS023 only for A-TEST

SPI ROM	Vender	Size	Quanta P/N	Vender P/N
Skylake 3.3V	WND	8M	AKE3EFP0N07	W25Q64FVSSIQ
	GGD	8M	AKE2EZN0Q00	GD25B64CSIGR

PCH SPI ROM(8M+4M)

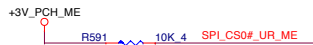
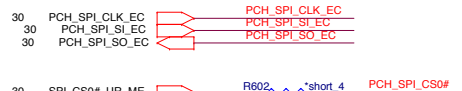
15ohm CS01502JB12

33ohm CS03302JB29

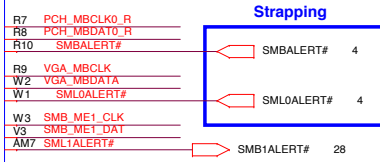


3.3K is original and for no support fast read function

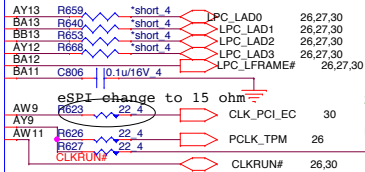
reserve for SPI fast read



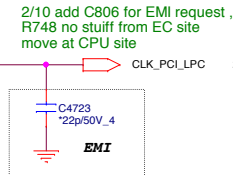
Strapping



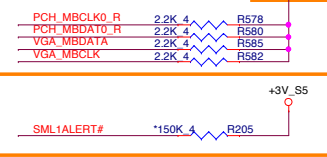
eSPI change to 15 ohm ckl v0.71 p.24



eSPI change to 15 ohm



SMBus



Termination Resistor Requirement for PCH PCHHOT# Pin Reserve PU 150K resistor

SMBus(PCH)

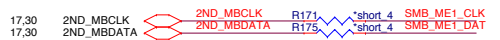
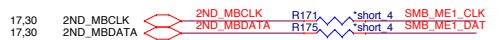
S5

PCH_XDP_WLAN/S5

SMBus(EC)

EC/S5

EC/S5

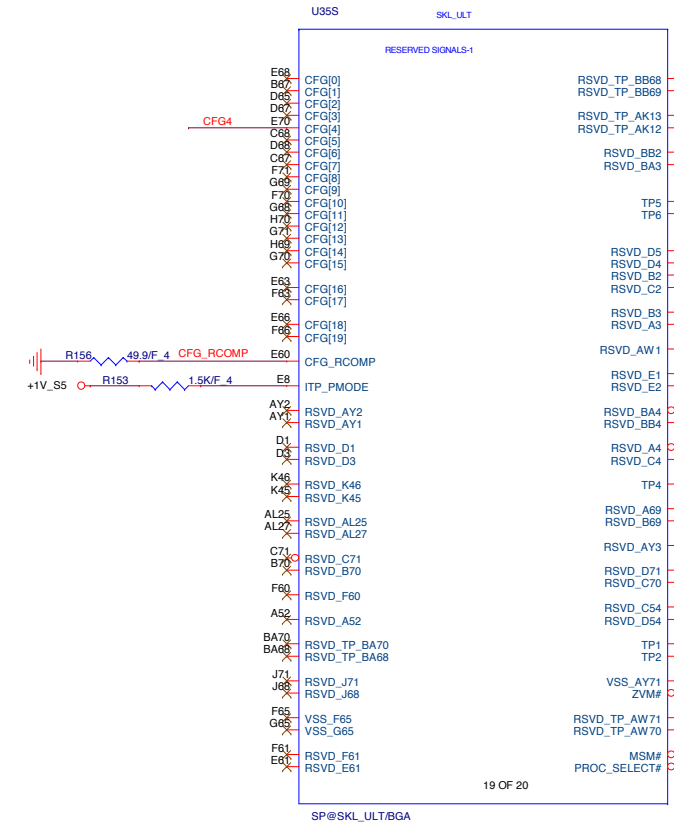


Quanta Computer Inc.

PROJECT : ZAA

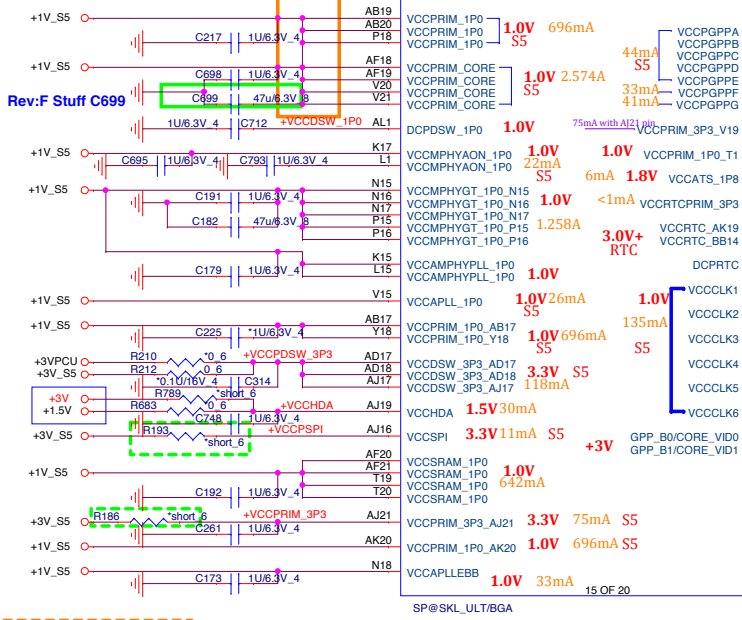
Size	Document Number	Rev
	Skylake 5 (SATA/HDA/SPI)	1A

Date: Monday, March 28, 2016 Sheet 7 of 48

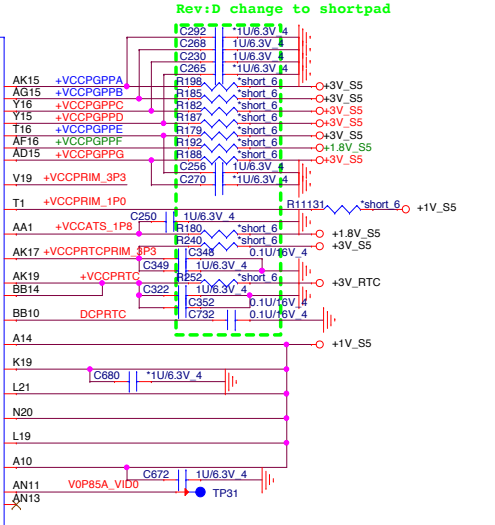


VCCPRIM_1P0 & VCCPRIM_CORE Short

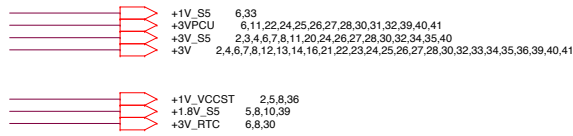
Rev:D change to shortpad
Rev:F Remove Short Jumper for all +1V_S5



GPIO Group Power Plane



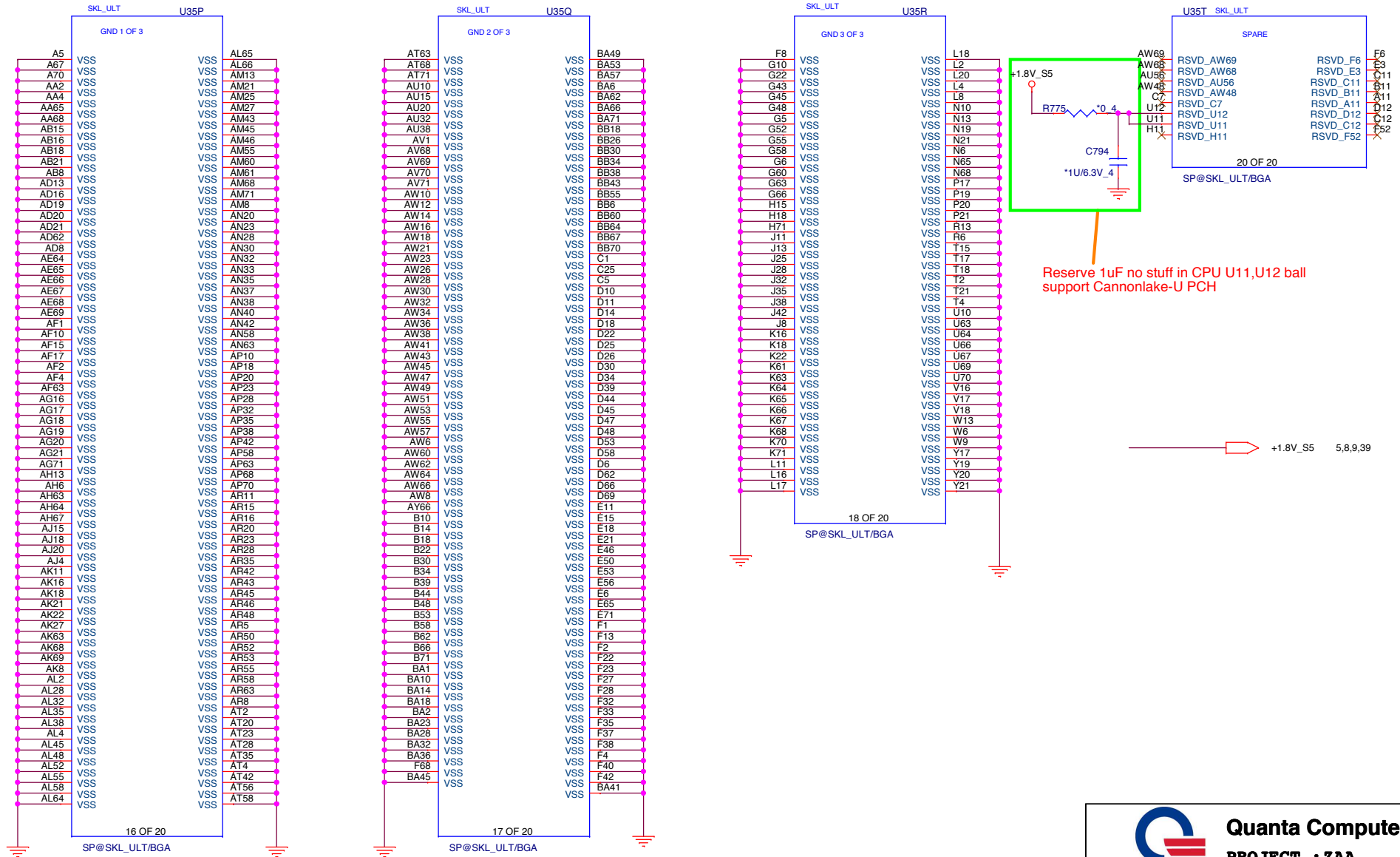
Pin Name	Strap description	Configuration	Note
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	1 = "Normal Operation; No stall (IPU 3K) 0 = Stall	
CFG[1]	Reserved Configuration lane		
CFG[2]	PCI Express* Static x16 Lane Numbering Reversal	1 = "Normal Operation(IPU 3K) 0 = Lan number reversed	H & S processor used only
CFG[3]	Reserved Configuration lane		
CFG[4]	eDP enable	1 = Disabled (IPU 3K) 0 = "Enabled	
CFG[6:5]	PCI Express* Bifunction	00 = 1x8, 2x4 PCI Express* 01 = reserved 10 = 2x8 PCI Express* 11 = 1x16 PCI Express*	H & S processor used only
CFG[7]	PEG Training	1 = "PEG Train immediately follow RESET# de-assertion (IPU 3K) 0 = PEG wait for BIOS for training	H & S processor used only
CFG[19:8]	Reserved Configuration lane		



Quanta Computer Inc.
PROJECT : ZAA

Size	Document Number	Rev
	SkyLake PCH-LP 15/19 (POWER)	1A
Date	Monday, March 28, 2016	Sheet 9 of 48

Skylake ULT (GND)

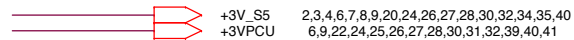
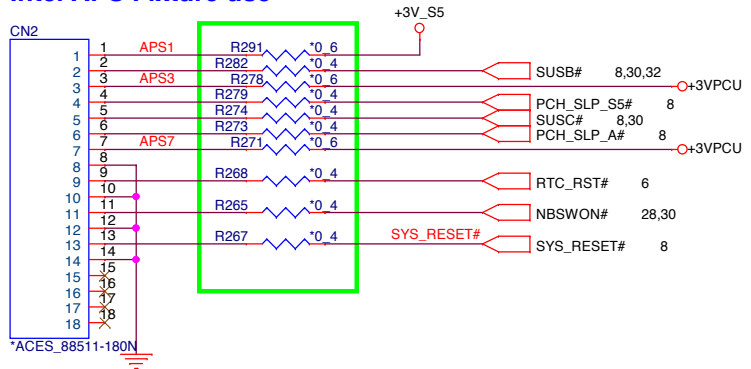


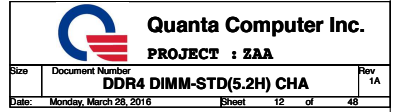
Quanta Computer Inc.
PROJECT : ZAA

Size	Document Number	Rev
	Skylake 10/17/18 (GND)	1A
Date:	Monday, March 28, 2016	Sheet 10 of 48

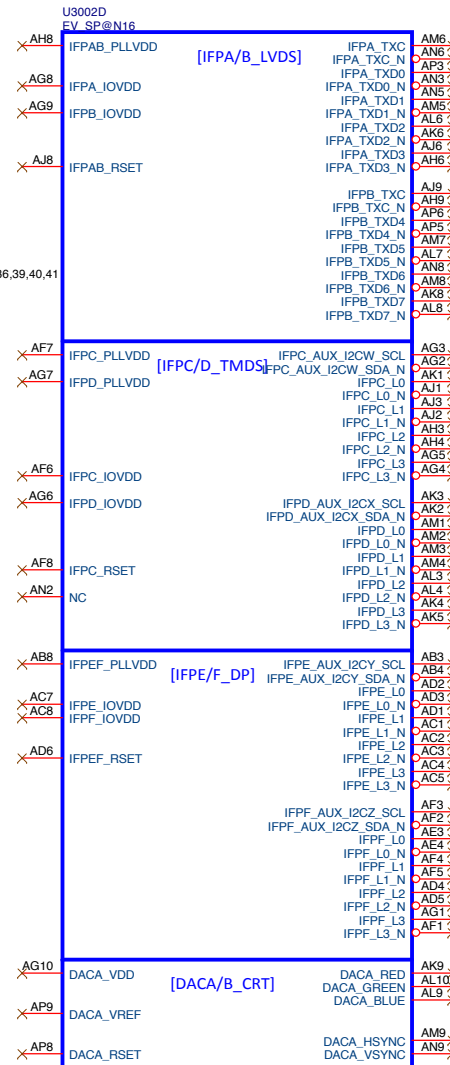


Intel APS Fixture use

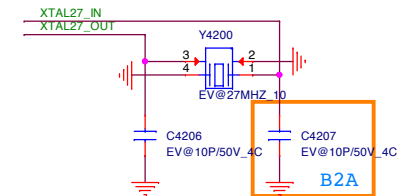
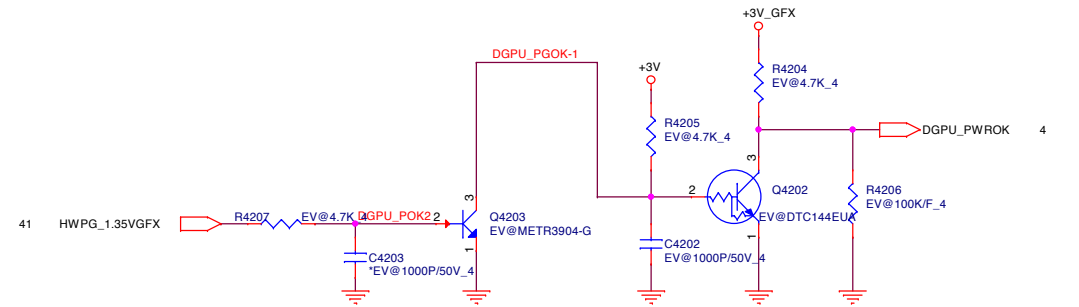
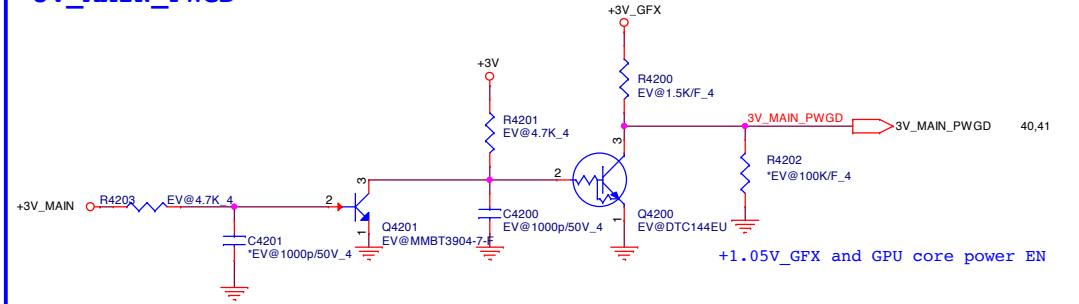




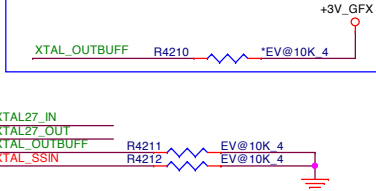
+3V_MAIN 14,15,17
 +1.05V_GFX 14,15,41
 +3V_GFX 14,17,30,41
 +3V 2,4,6,7,8,9,12,13,14,21,22,23,24,25,26,27,28,30,32,33,34,35,36,39,40,41



3V_MAIN_PWGD

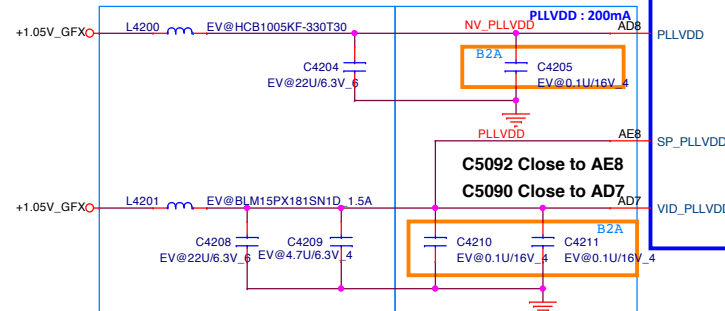


Reserve

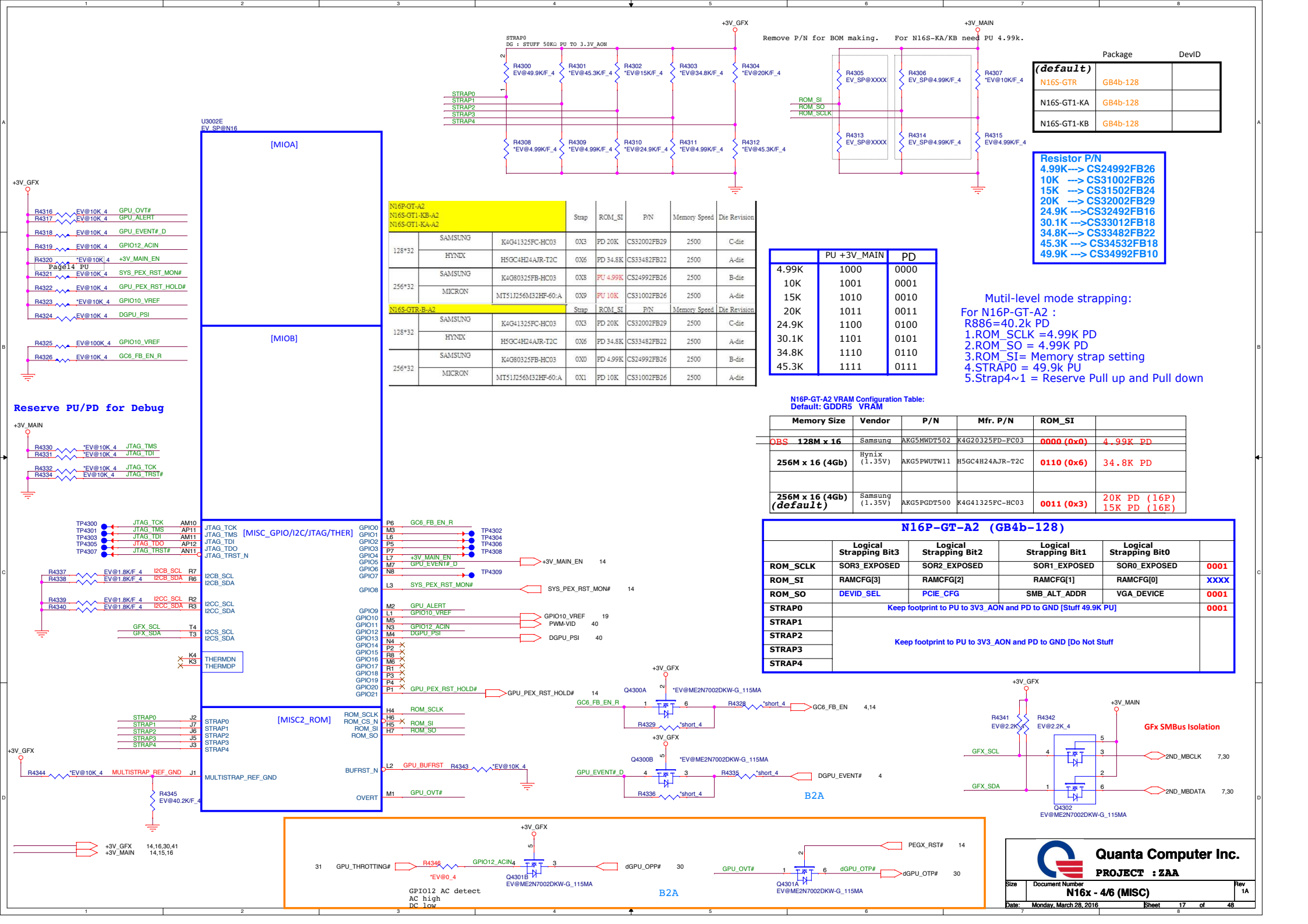


PLACE CLOSE TO GPU

PLACE CLOSE TO BALLS



Quanta Computer Inc.
PROJECT : ZAA



VDD/XVDD : 43A

+VGPU_CORE

U3002F
EV_SP@N16

[GPU VDD]

+VGPU_CORE

U3002G
EV_SP@N16

[GPU GND]

+VGPU_CORE

PLACE UNDER GPU

PLACE NEAR GPU



Quanta Computer Inc.

PROJECT : ZAA

CHANNEL A: 1024MB GDDR5x32

Non-mirror, MF=0
Channel A
<0-31>

Mirror, MF=1
Channel A
<32-63>

Non-mirror, MF=0
Channel B
<0-31>

Mirror, MF=1
Channel B
<32-63>

DQA24-31

DQA16-23

DQA8-15

DQA0-7

DQA32-39

DQA40-47

DQA48-55

DQA56-63

DQB24-31

DQB16-23

DQB8-15

DQB0-7

DQB32-39

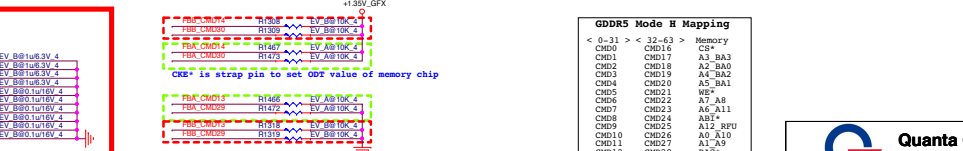
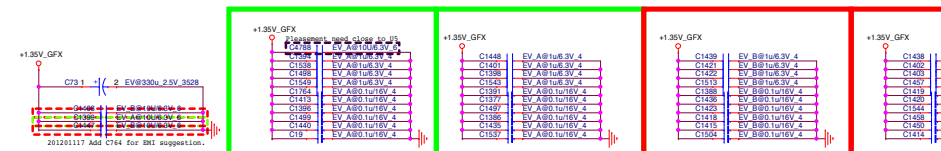
DQB40-47

DQB48-55

DQB56-63

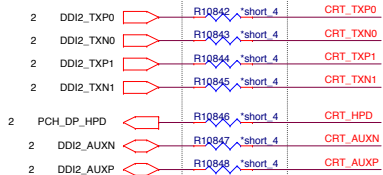
KB OnlyA

KA OnlyB

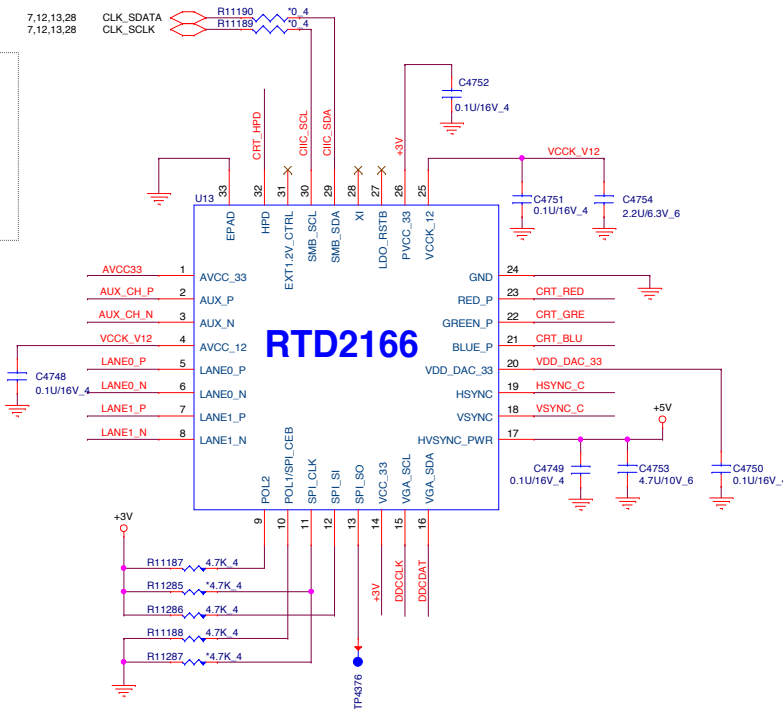
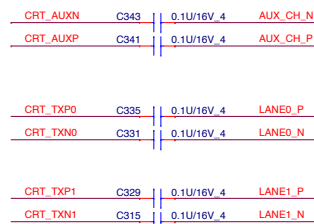


DP TO VGA

Close to CPU side of CAP.



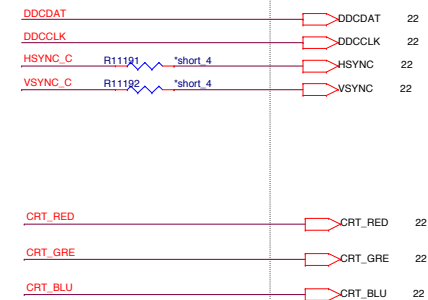
Power



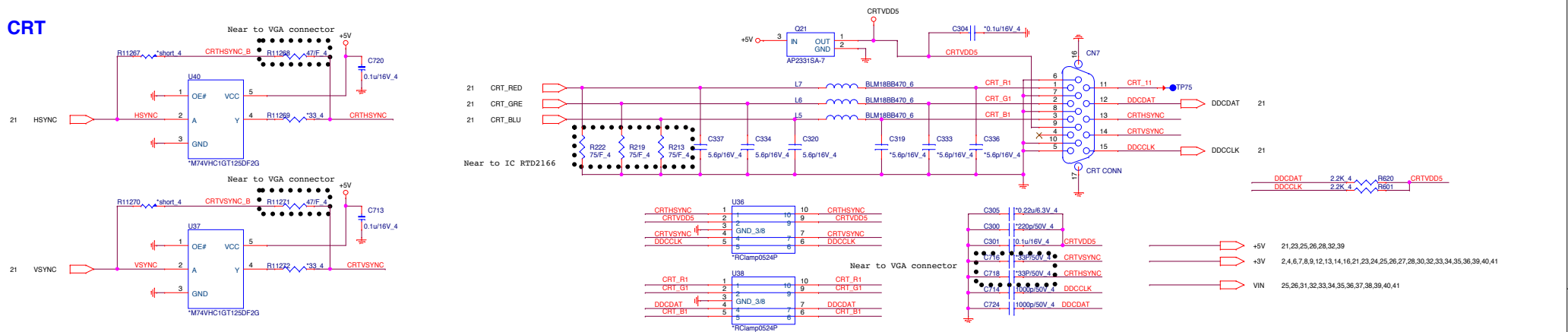
Note:

- 1- C1,C3,C4,C5,C11,C16, C21 should be placed close to chip
- 2- C5 shold be X5R material
- 3- R6, R7, R8 should be 75 ohm with +/-1%
- 4- Suggest to connect Pin 29 and Pin 30 to PCH SMBUS for debug purpose.
- 5- This configuration is for internal ROM mode and using embedded LDO mode.

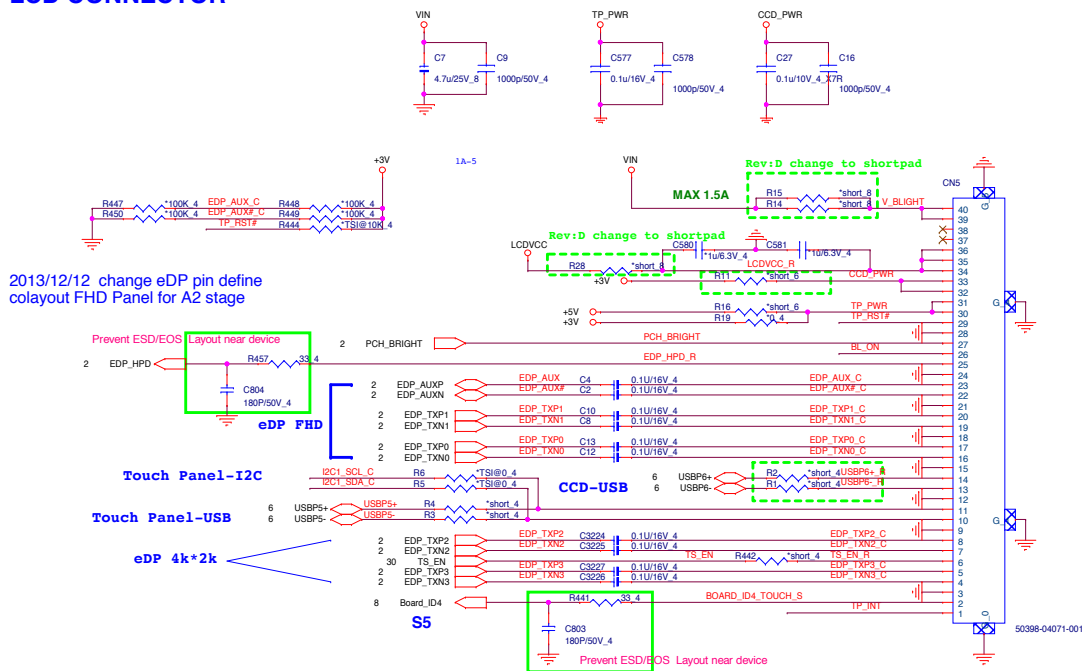
VGA



CRT



LCD CONNECTOR



2013/12/12 change eDP pin define
colayout FHD Panel for A2 stage

Prevent ESD/EOS Layout near dev

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Touch Panel-I2C

Touch Panel-USB

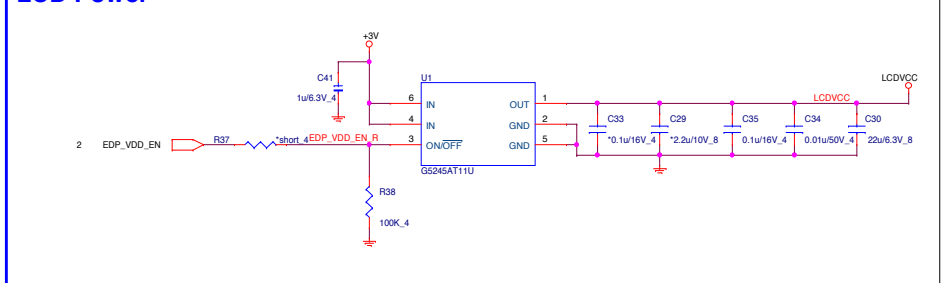
eDP 4k*2k \triangleleft

1C1-2 2

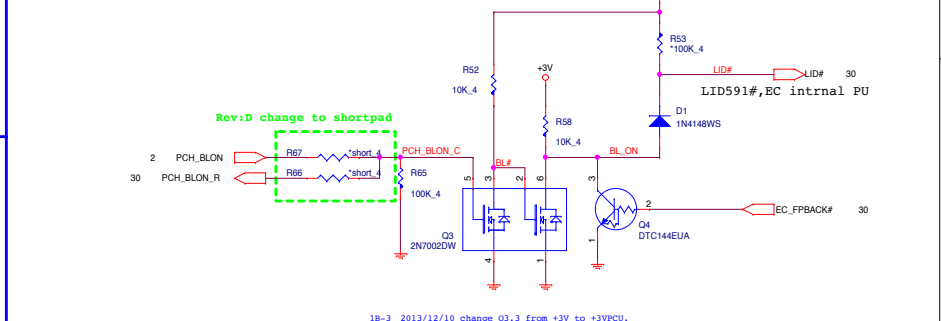
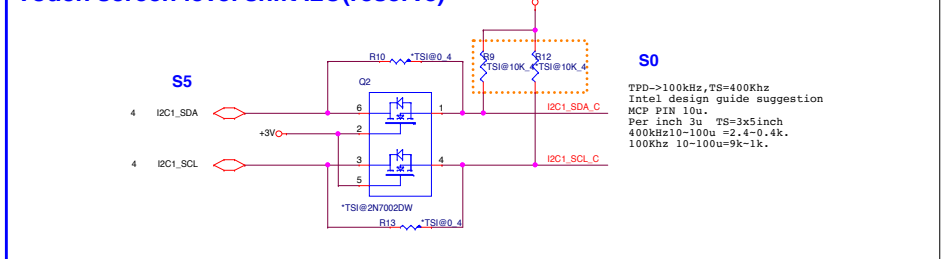
Tough Paper

4. TR INT RCH ☒

LCD Power



Touch screen level shift I2C(reserve)

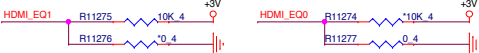


1B-3 2013/12/10 change 03.3 from +3V to +3VPCU.

1st:AL009249000 -- BCD
2nd:AL009132001 -- ANC

HDMI

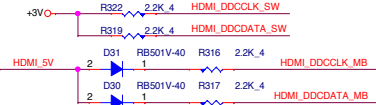
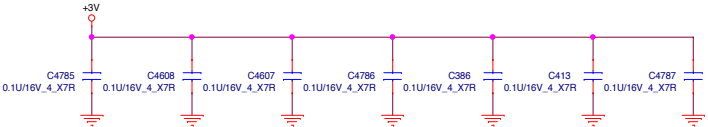
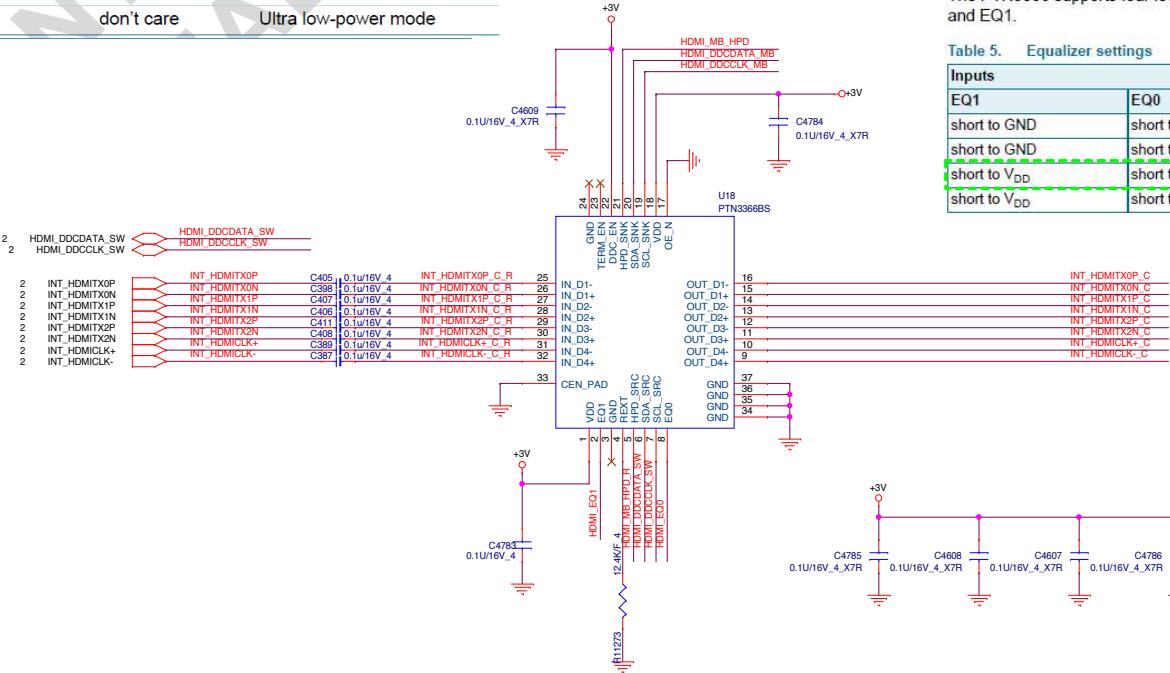
OE_N	DDC_EN	HPD_SINK	Source output	PTN3366 power mode
LOW	HIGH	HIGH	source active	Active mode; DDC active
LOW	LOW	LOW	don't care	Standby mode
HIGH	LOW	don't care	don't care	Ultra low-power mode



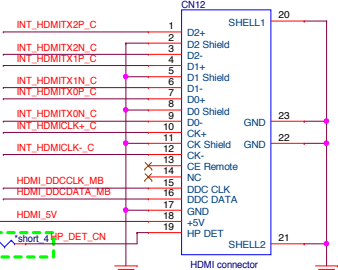
The PTN3366 supports four level equalization settings based on binary input pins EQ0 and EQ1.

Table 5. Equalizer settings		
Inputs		Equalization for 3 Gbit/s
EQ1	EQ0	
short to GND	short to GND	0 dB
short to GND	short to VDD	2 dB
short to VDD	short to GND	4 dB
short to VDD	short to VDD	6 dB

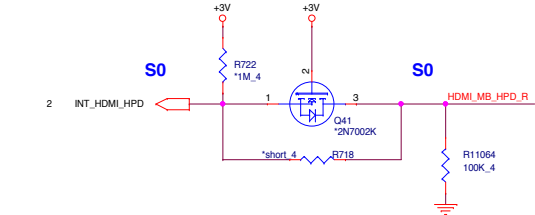
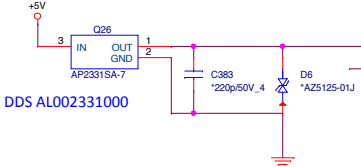
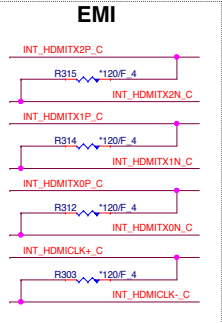
From PCH



HDMI connector



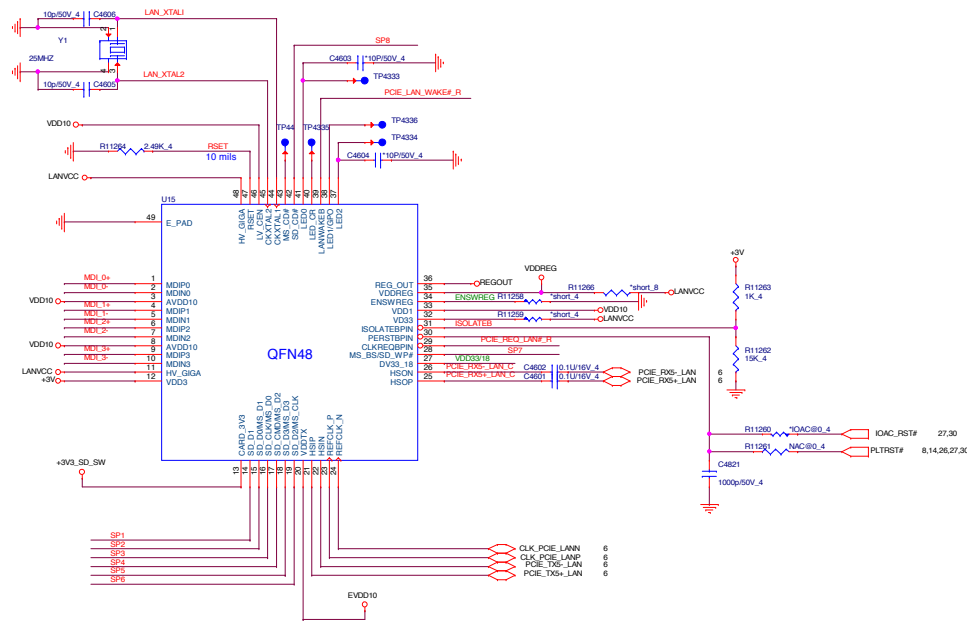
Rev:D change to shortpad



LAN & Card reader Combo (LAN)

+3V 2,4,6,7,8,9,12,13,14,16,21,22,23,25,26,27,28,30,32,33,34,35,36,39,40,41
+3VPCU 6,9,11,22,25,26,27,28,30,31,32,39,40,41
+3V_S5 2,3,4,6,7,8,9,11,20,26,27,28,30,32,34,35,40

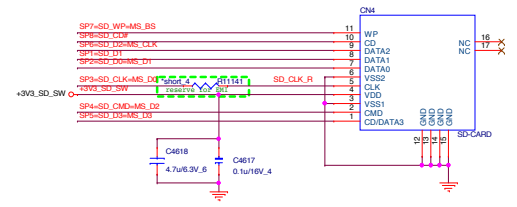
Giga LAN (LAN)



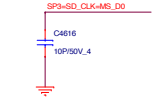
Card Reader (CRD)

SP1	R11254	short_4	SP1-SD_D1
SP2	R11254	short_4	SP2-SD_D0MS_D1
SP3	R11254	short_4	SP3-SD_CMDMS_D2
SP4	R11254	short_4	SP4-SD_CMDMS_D3
SP5	R11254	short_4	SP5-SD_CMDMS_D4
SP6	R11254	short_4	SP6-SD_CMDMS_D5
SP7	R11254	short_4	SP7-SD_CMDMS_D6
SP8	R11254	short_4	SP8-SD_CMDMS_D7

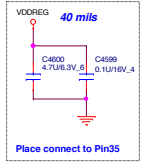
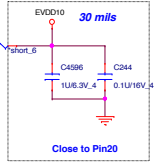
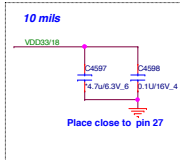
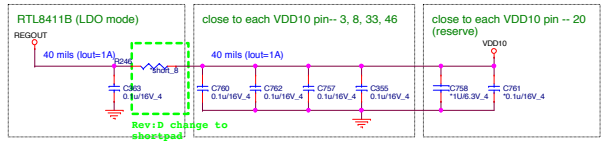
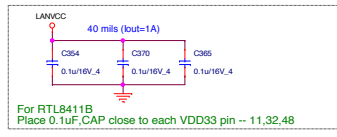
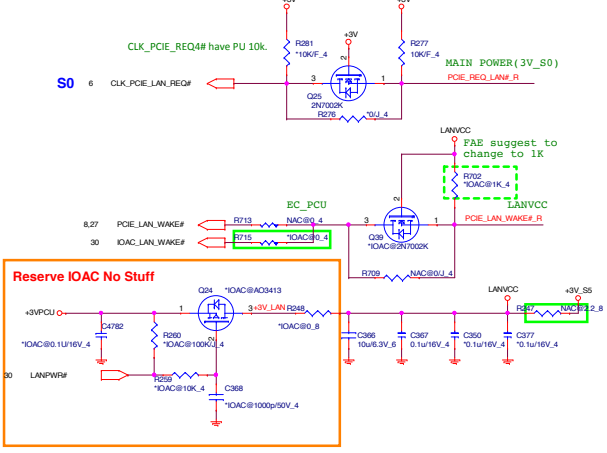
Share Pin	SD_D1	SD_D0	MS_D1
SP1	SD_D1	SD_D0	MS_D1
SP2	SD_D1	SD_D0	MS_D1
SP3	SD_D1	SD_D0	MS_D1
SP4	SD_D1	SD_D0	MS_D1
SP5	SD_D1	SD_D0	MS_D1
SP6	SD_D1	SD_D0	MS_D1
SP7	SD_D1	SD_D0	MS_D1
SP8	SD_D1	SD_D0	MS_D1



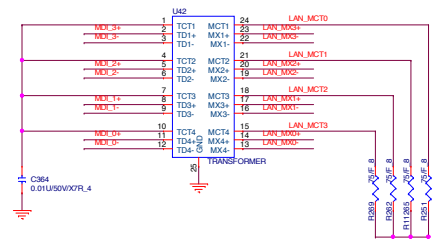
EMI



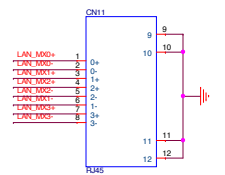
Leakage circuit (MPC)



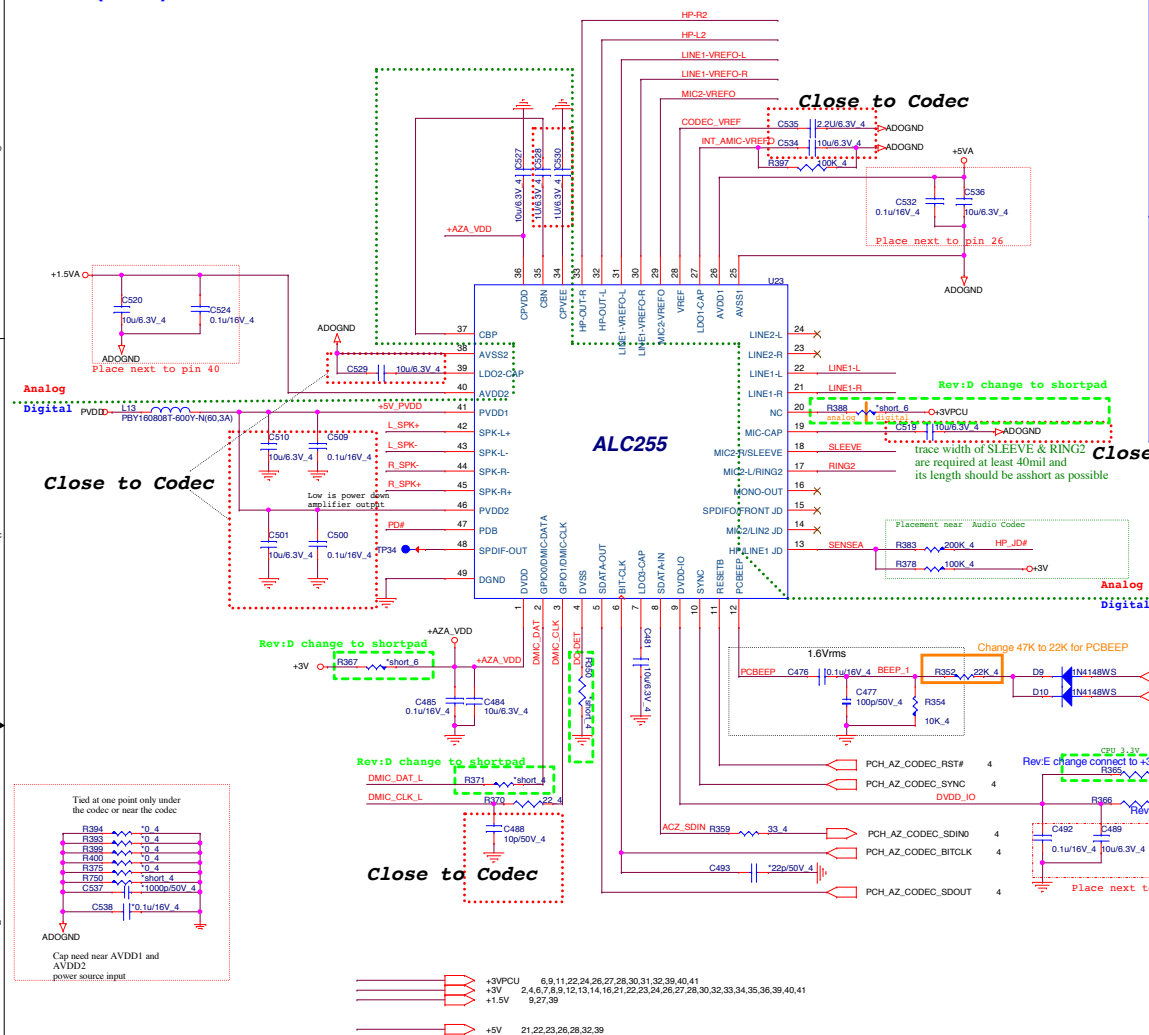
Transformer



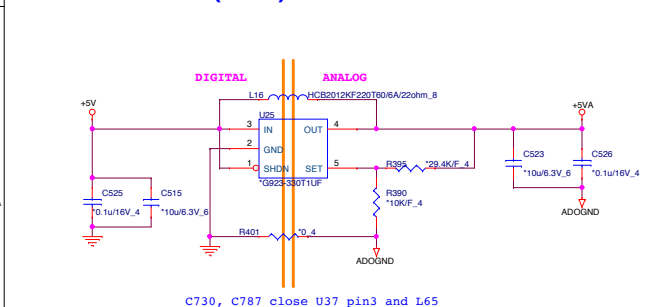
RJ45 Connector



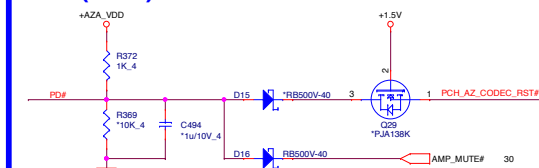
Codec(ADO)



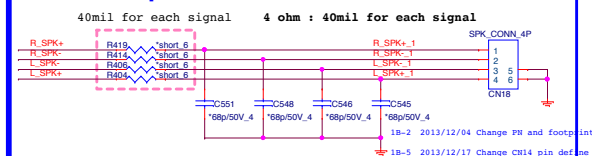
Codec PWR 5V(ADO)



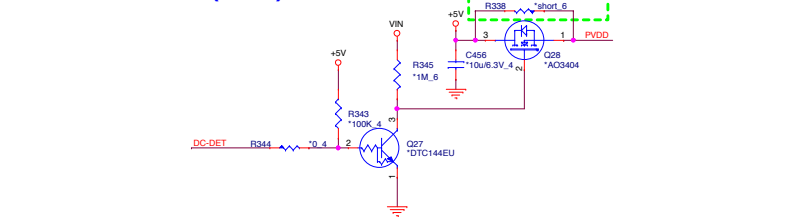
Mute(ADO)



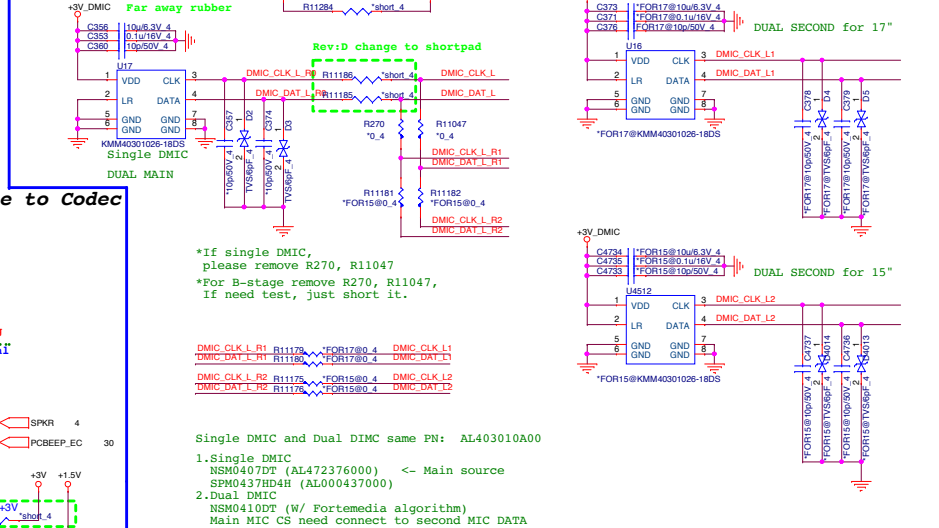
Internal Speaker



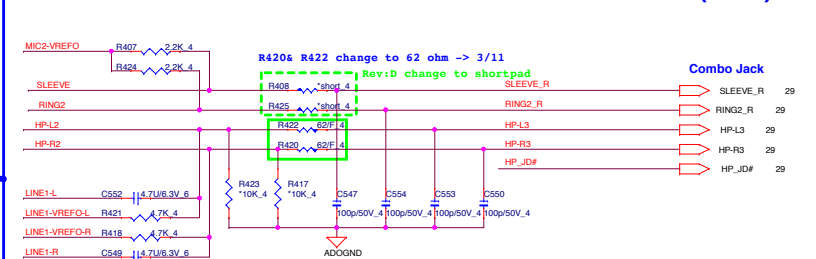
DC-DET circuit(ADO)



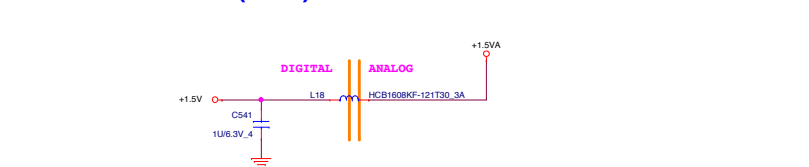
D-Mic (MIC)



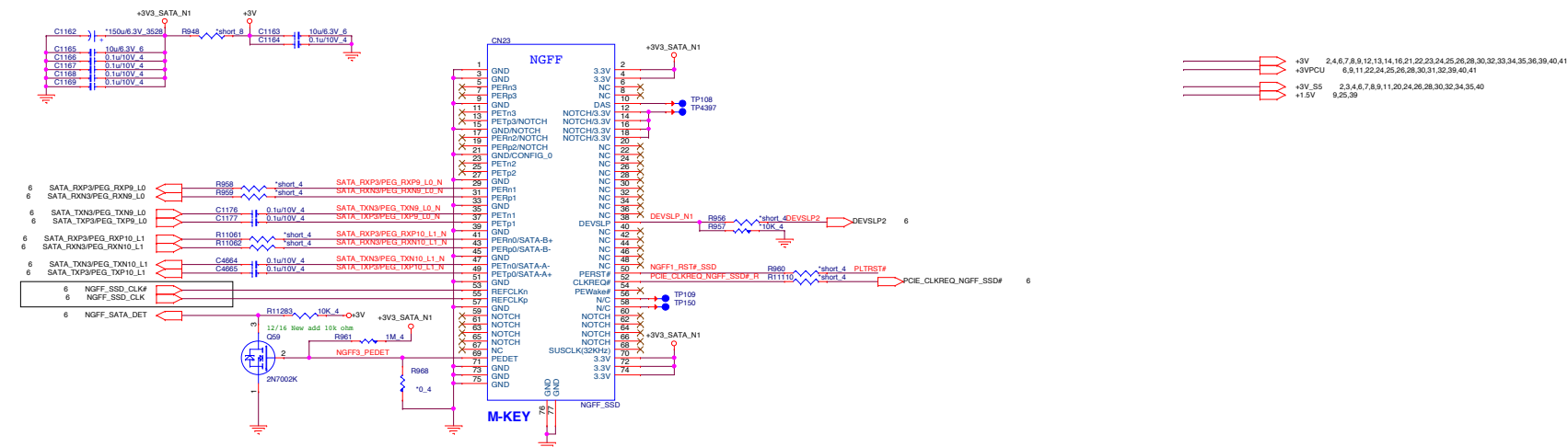
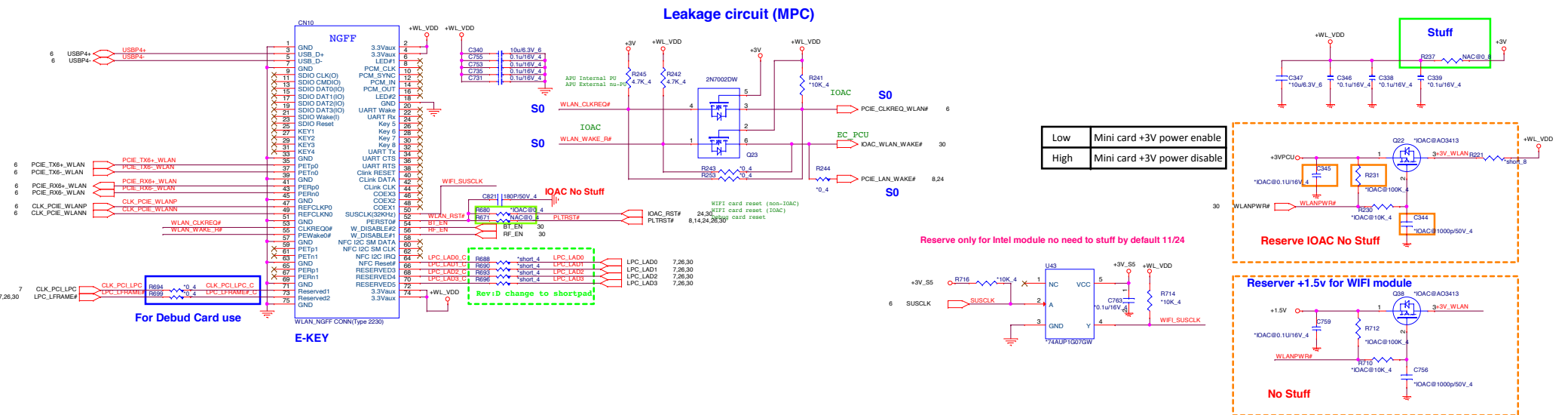
Universal Audio Jack HEADPHONE/MIC/LINE combo (ADO)



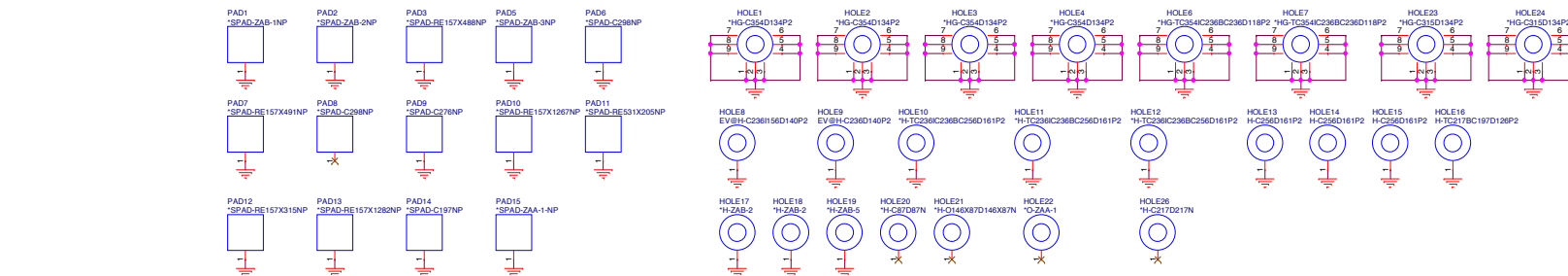
Codec PWR 1.5V(ADO)



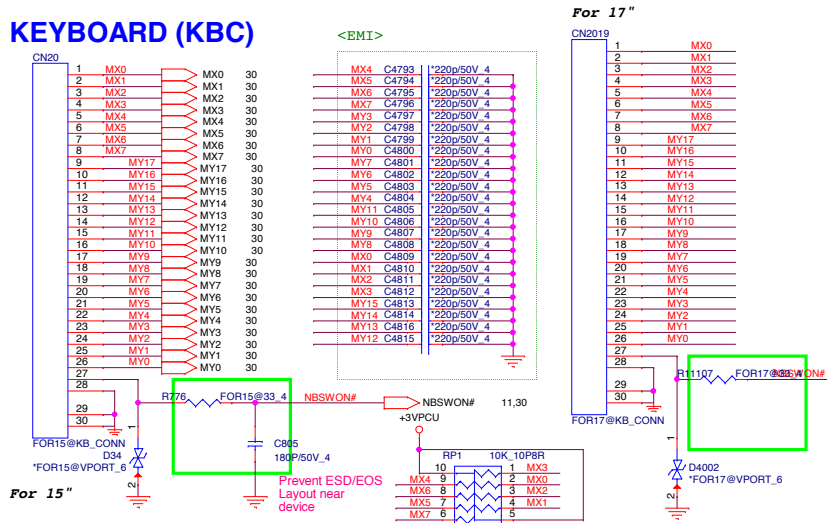
NGFF_M.2 WiFi & BT (NGF)



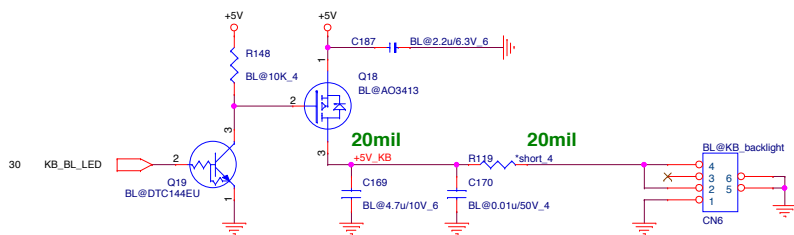
PAD and HOLE



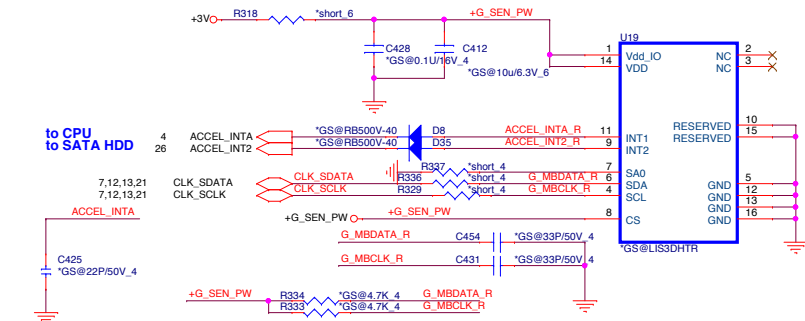
KEYBOARD (KBC)



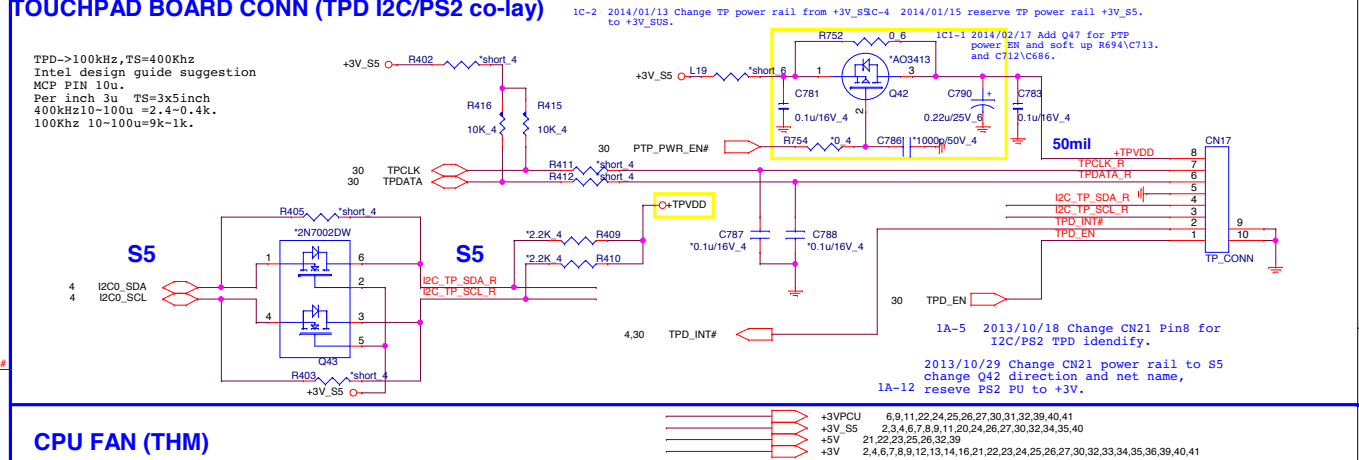
KB_BL LED (KBC)



G-sensor(ACS)

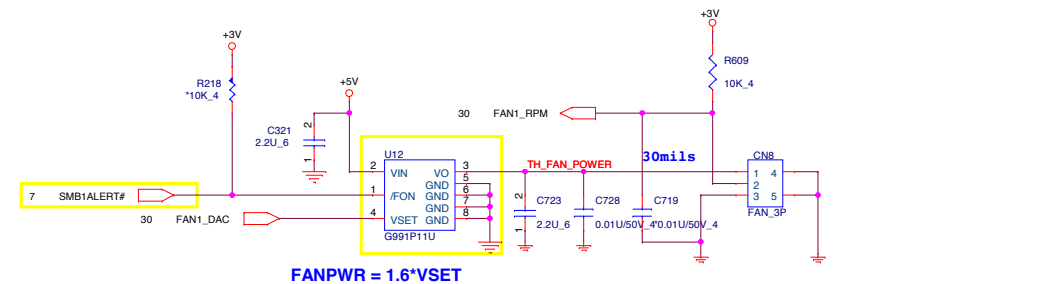


TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)

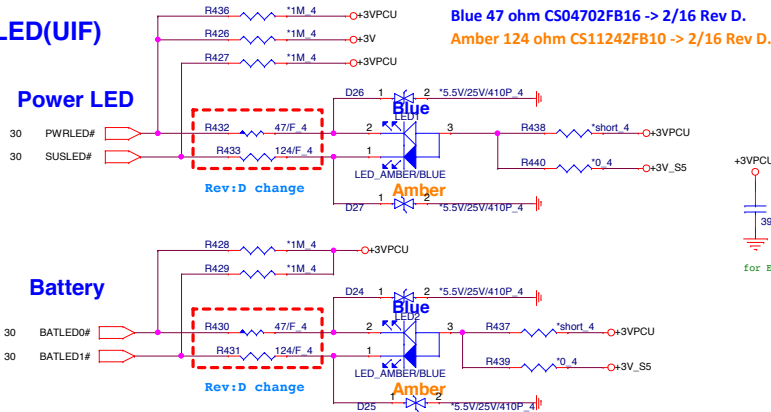


CPU FAN (THM)

Prevent ESD/EOS
Layout near
device



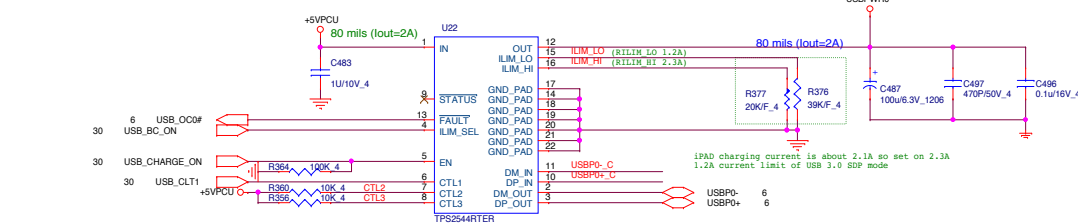
POWER LED(UIF)



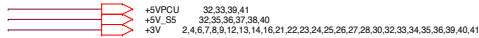
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	KB/TP/FAN	1A
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USB Charger to 3.0 (UBC)



TI:AL002544001(TPS2544)
Silergy: AL055544000 (SLGC55544VTR)



	CTL1	CTL2	CTL3	ILIM_SEL
SDP	1	1	1	0
CDP	1	1	1	1
DCP	0	1	1	X

RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:

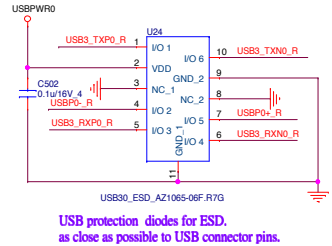
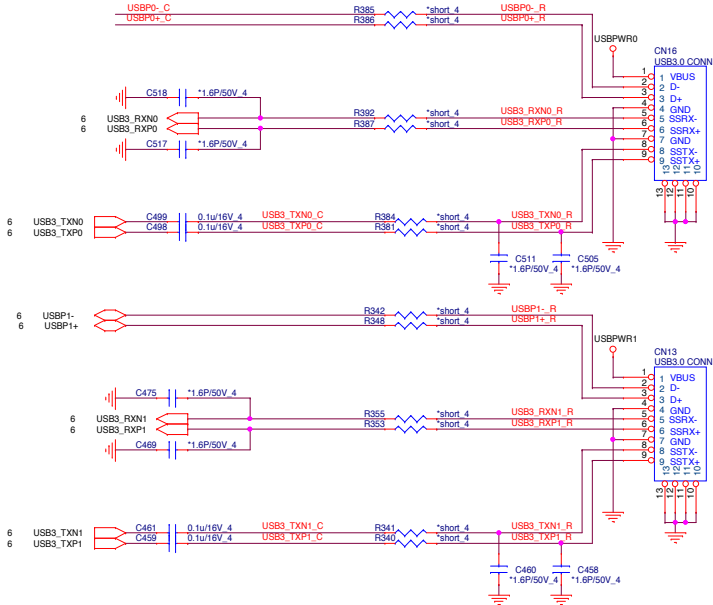
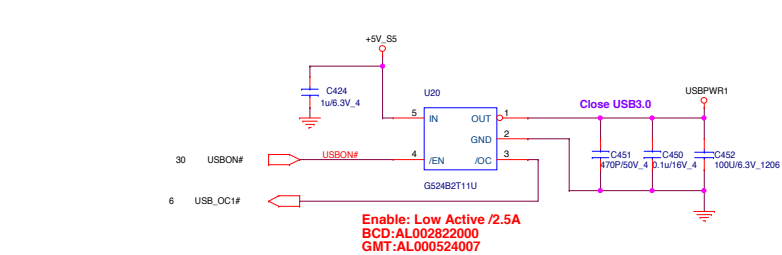
1. ILIM_SEL is always set high
 2. Load Detection - Port Power Management is not used
 3. Mouse / Keyboard wake function is not used
- If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.

The following equation programs the typical current limit:

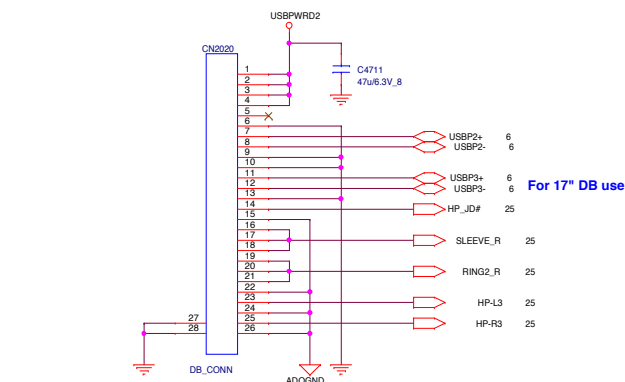
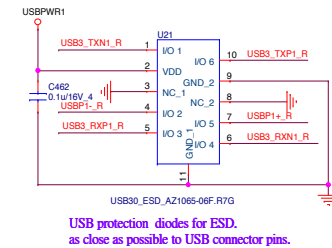
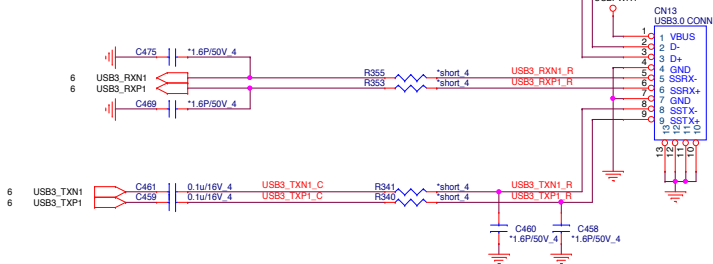
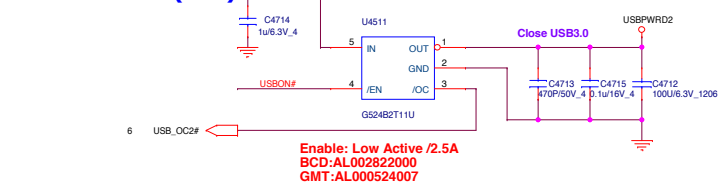
(1)
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

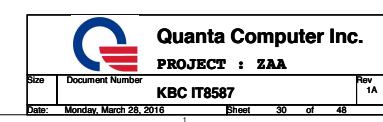
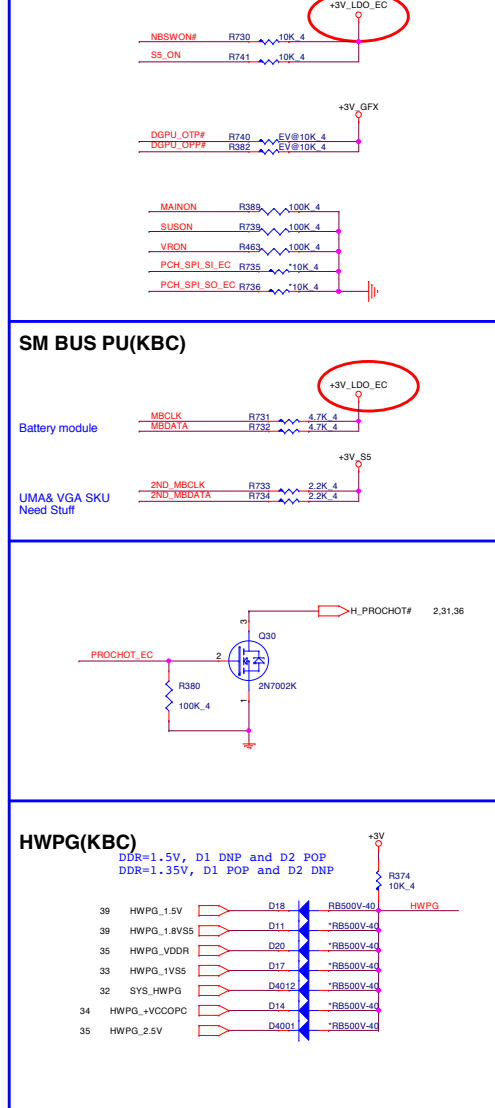
$$IOS_typ(mA) = 50,250 / (RILIM_XX(K\Omega) + 0.1)$$

USB 3.0 Connector (UB3)



USB2.0 DB (UB2)

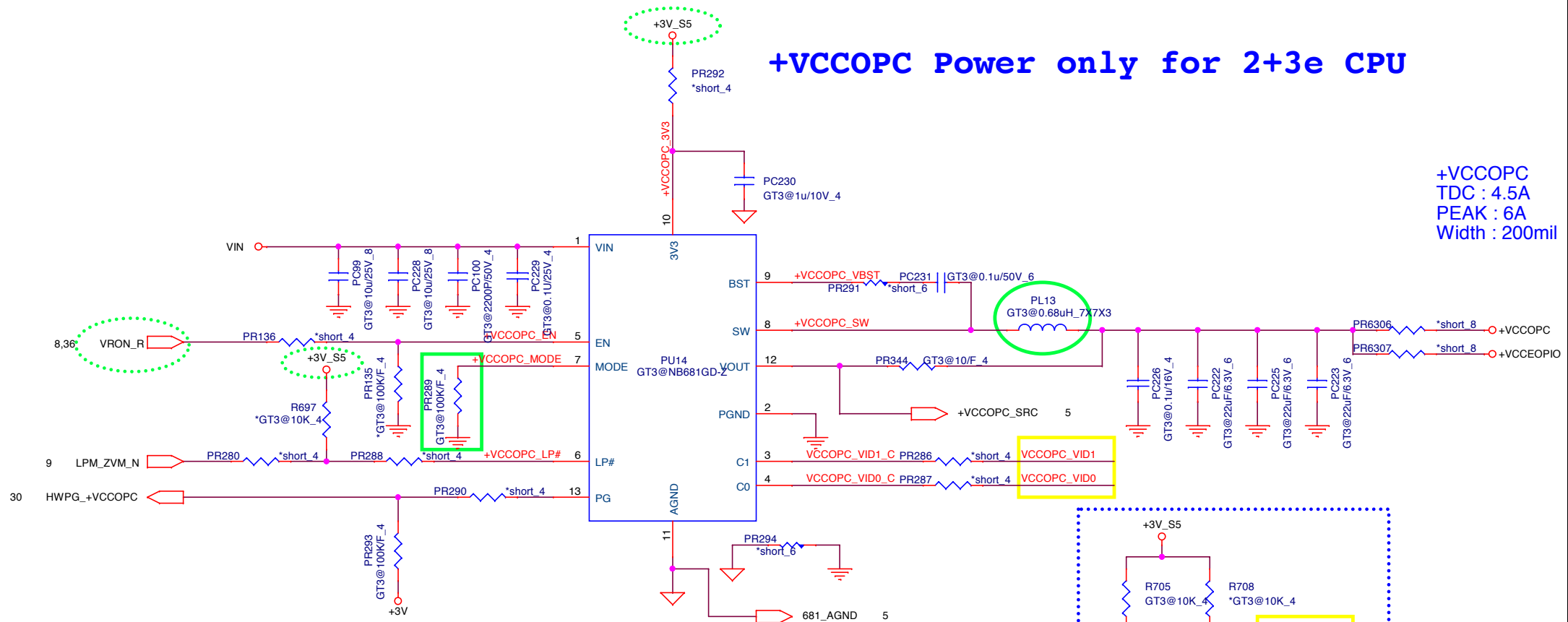






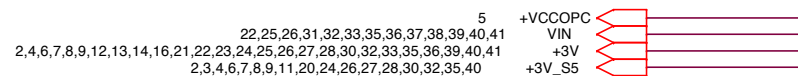
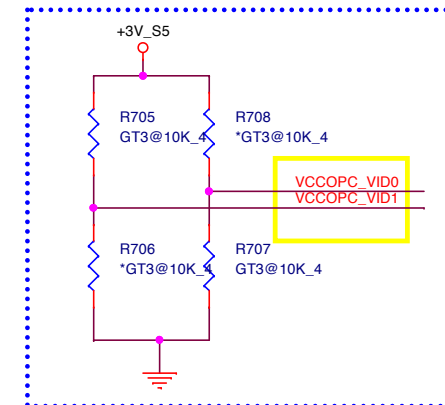
+VCCOPC Power only for 2+3e CPU

+VCCOPC
TDC : 4.5A
PEAK : 6A
Width : 200mil



Mode	VR Rail
0 ohm	VCCIO
Floating	PRIMCORE
100K	EDRAM/EOPIC
150K	Other

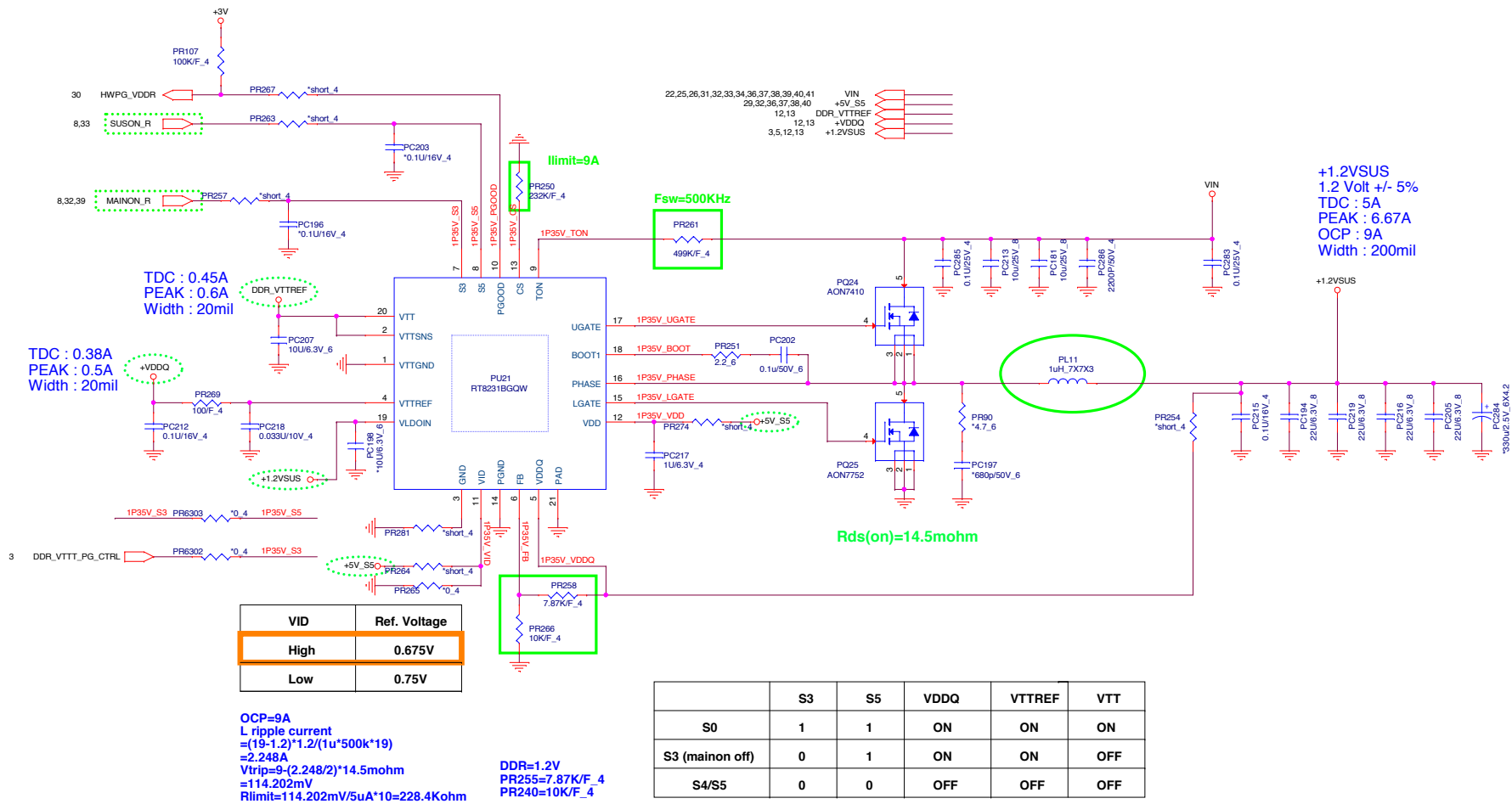
	LP#	C1	C0	Vo
VCCEDRAM	0	X	X	0V
	1	0	0	0.8V(MSM)
	1	0	1	0.95V
	1	1	0	1.0V
	1	1	1	1.05V



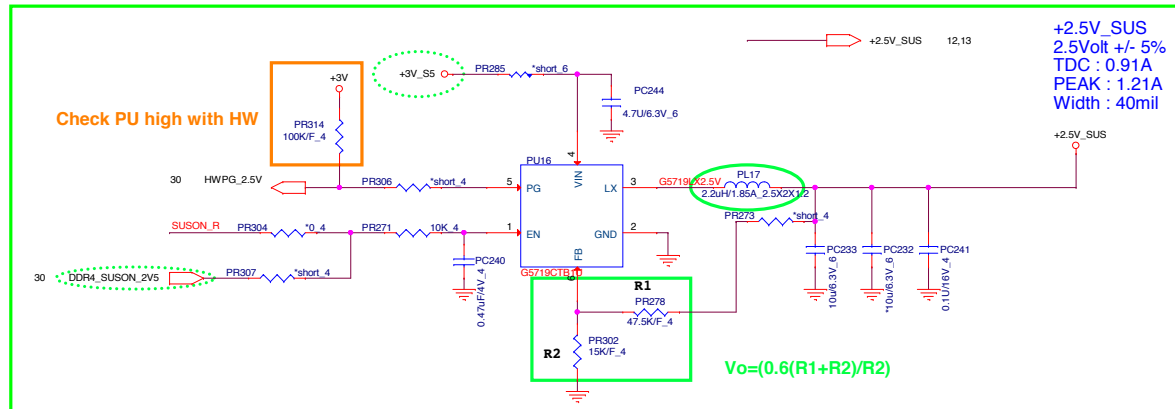
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Size: Document Number: **+VCCOPC (NB681GD-Z)** Rev 1A

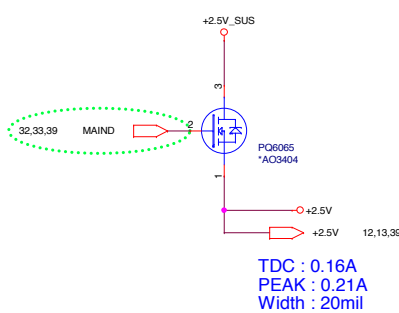
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+2.5VSUS Power Rail For DDR4



10/26 Reserve +2.5V for DDR4 VDDSPD



ZAAA 6L power solution table

GT2 : PC134 CH4104K9B03 0.1uF/25V
GT2 : PR6301 CS00002JB38 0 ohm

GT2 : PR194 CS21912FB13 1.94K
GT2 : PR207 CS41622FB11 162K

GT2 : PR192 CS12672FB02 267
GT2 : PR203 CS37872FB15 78.7K
GT2 : PR198 CS38872FB18 88.7K

GT3 : PC134 CH4152K9B02 0.15uF/10V
GT3 : PR6301 Unstuff

GT3 : PR194 CS22552FB01 2.55K
GT3 : PR207 CS41402FB14 140K

GT3 : PR192 CS13402FB00 340
GT3 : PR203 CS38872FB18 88.7K
GT3 : PR198 CS39312FB15 93.1K

GT2 : PR19 Unstuff
GT2 : PC17 Unstuff
GT2 : PC18 Unstuff

GT3 : PR18, PR19, PR188 CS41003F932 100K
GT3 : PR203 CH3224K1B01 0.022U/25V
GT3 : PC18 CH3224K1B01 0.022U/25V

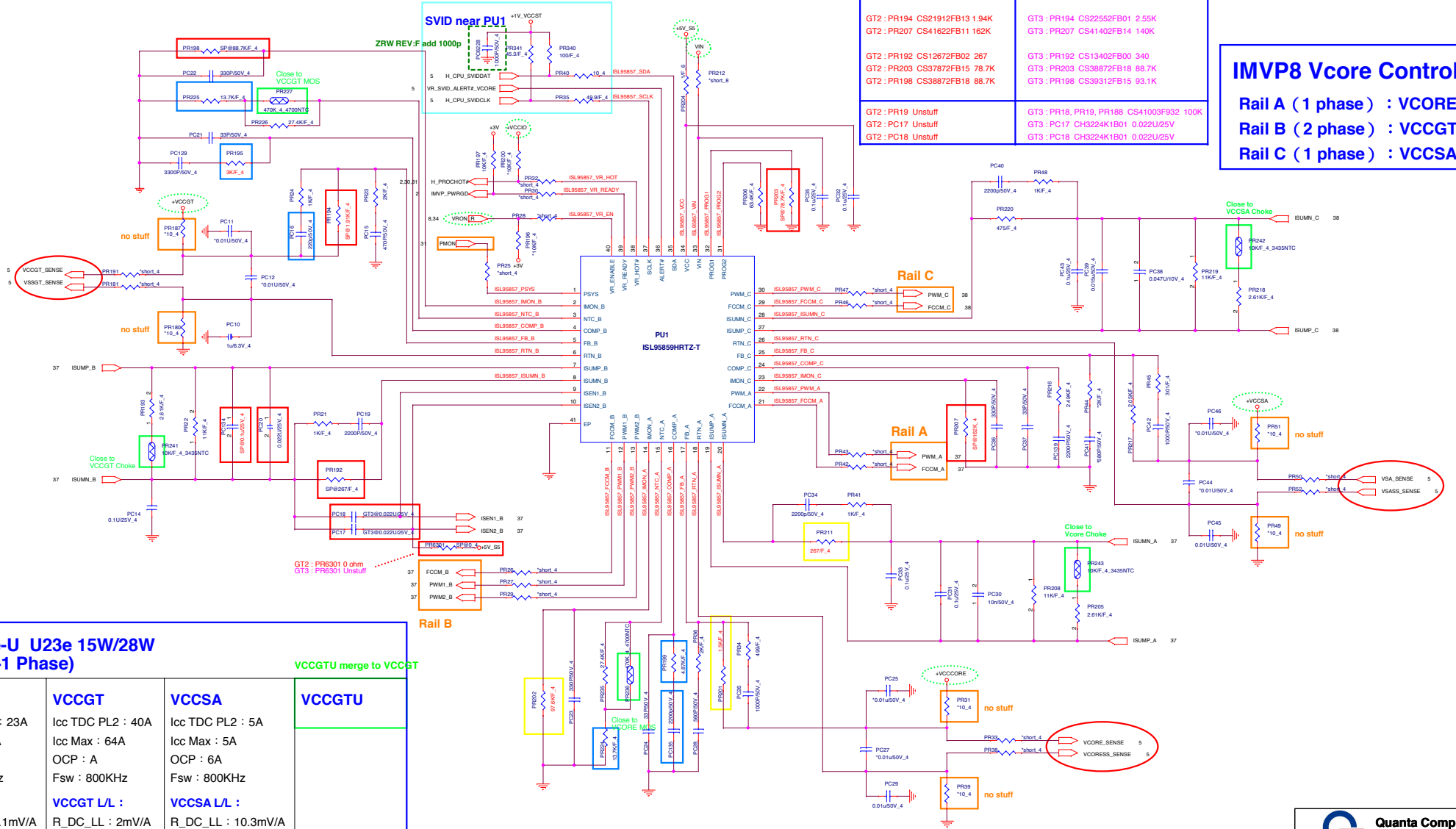
IMVP8 Vcore Controller

Rail A (1 phase) : VCORE
Rail B (2 phase) : VCCGT
Rail C (1 phase) : VCCSA

Check PU high with HW

SVID near PU1

ZRW REV-F add 1000p



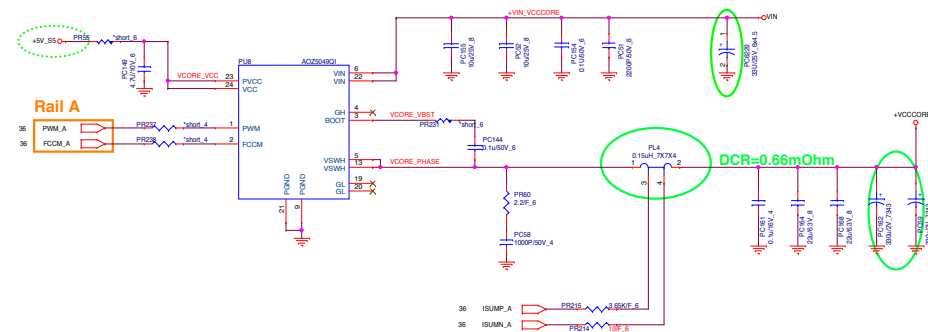
Skylake-U U23e 15W/28W (1+2+1+1 Phase)

VCORE	VCCGT	VCCSA	VCCGTU
Icc TDC PL2 : 23A	Icc TDC PL2 : 40A	Icc TDC PL2 : 5A	
Icc Max : 32A	Icc Max : 64A	Icc Max : 5A	
OCF : 35A	OCF : A	OCF : 6A	
Fsw : 800KHz	Fsw : 800KHz	Fsw : 800KHz	
VCORE L/L :	VCCGT L/L :	VCCSA L/L :	
R_DC_LL : 2.1mV/A	R_DC_LL : 2mV/A	R_DC_LL : 10.3mV/A	
R_AC_LL : 2.1mV/A	R_AC_LL : 2mV/A	R_AC_LL : 10.3mV/A	

VCCGTU merge to VCCGT

GT2: PR19 Unstuff
GT3: PR19 CS41003F932 100K

VCORE



VCORE

Icc TDC PL2 : 23A

Icc Max : 32A

OCF : 35A

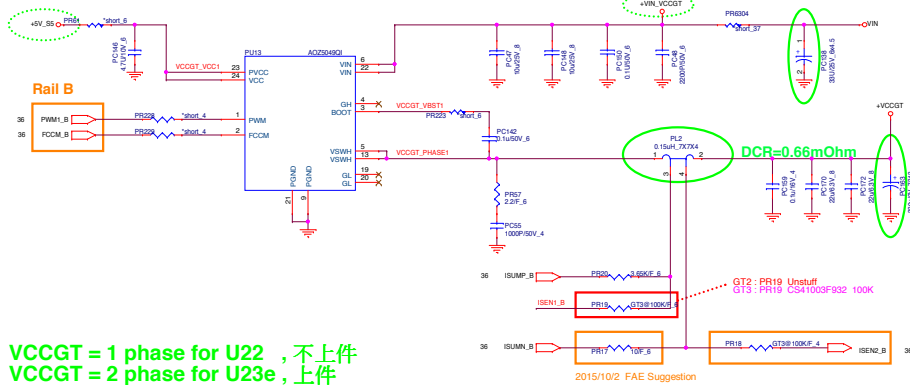
Fsw : 800KHz

VCORE LL :

R_DC_LL : 2.1mV/A

R_AC_LL : 2.1mV/A

VCCGT



VCCGT

Icc TDC PL2 : 40A

Icc Max : 64A

OCF : A

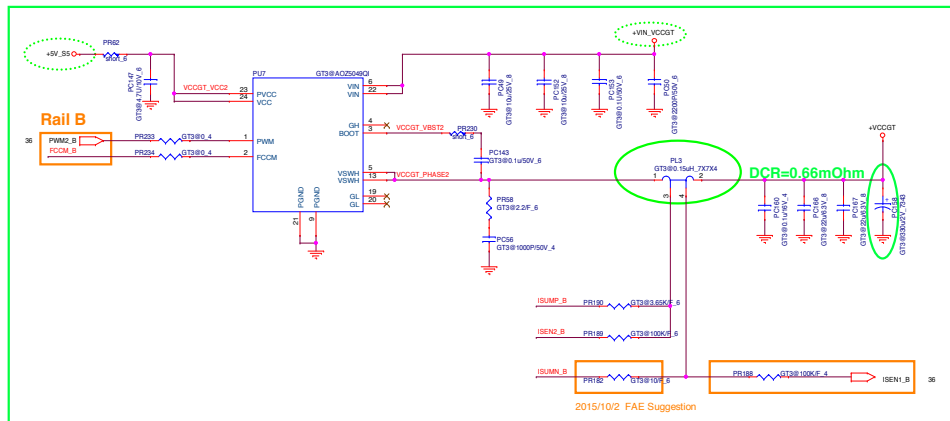
Fsw : 800KHz

VCCGT LL :

R_DC_LL : 2mV/A

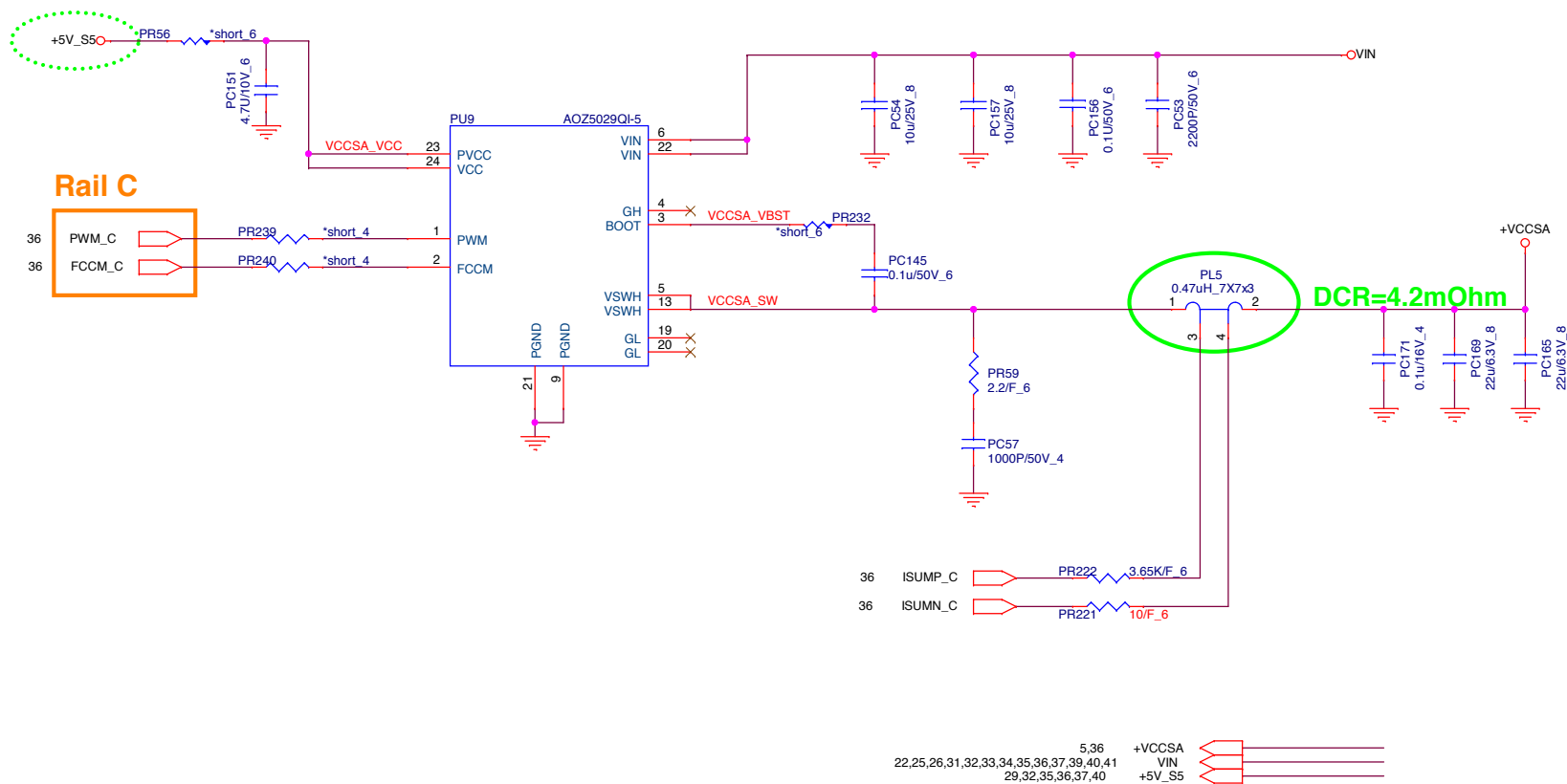
R_AC_LL : 2mV/A

VCCGT = 1 phase for U22 , 不上件
VCCGT = 2 phase for U23e , 上件



5,36 +VCCORE
22,25,26,31,32,33,34,35,36,38,39,40,41 VIN
5,36 +VCCGT
29,32,35,36,38,40 +V, 5S

VCCSA



VCCSA

Icc TDC PL2 : 5A

Icc Max : 5A

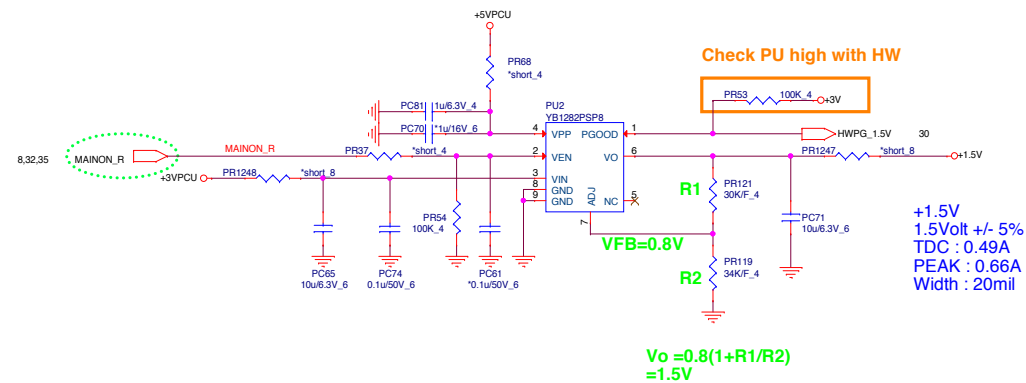
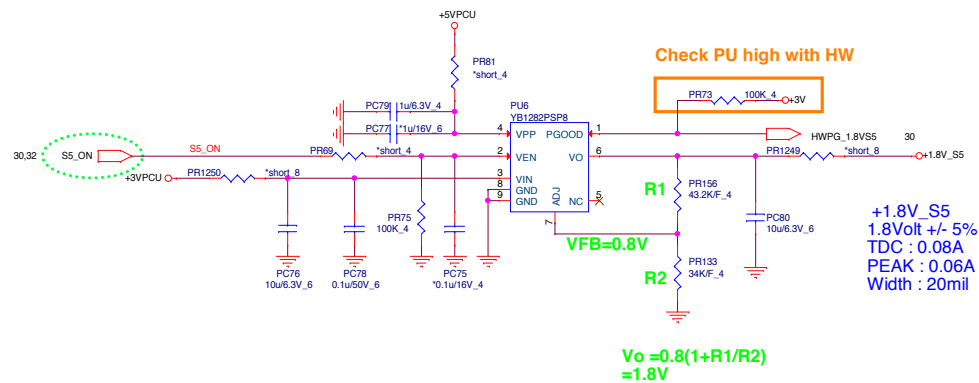
OCP : 6A

Fsw : 800KHz

VCCSA L/L :

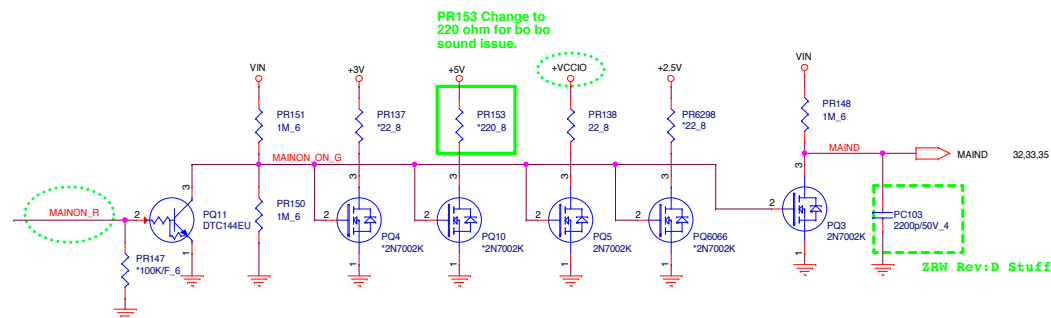
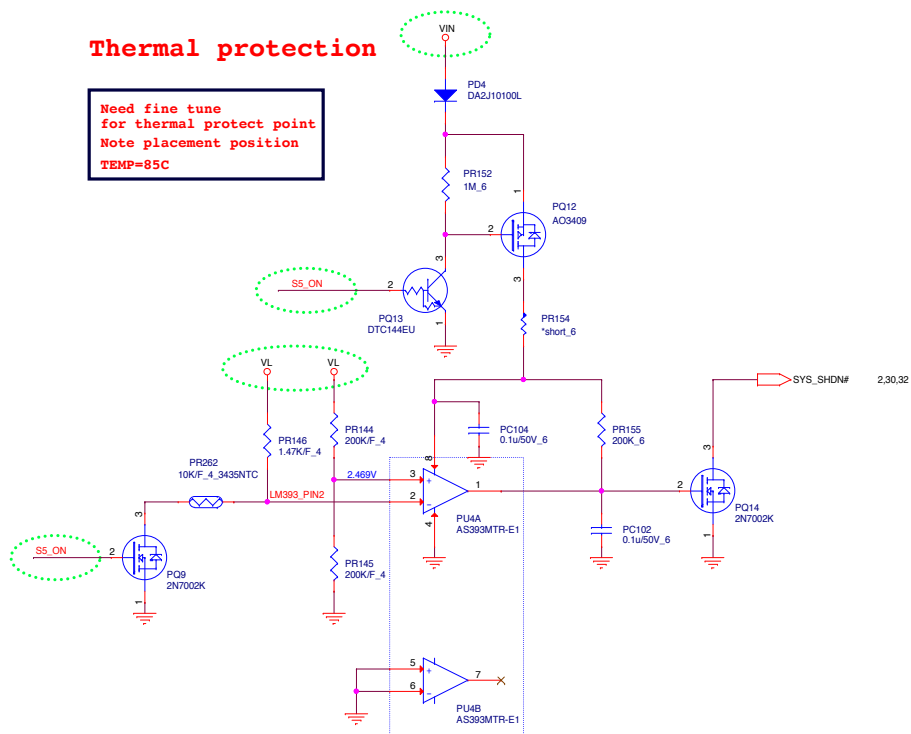
R_DC_LL : 10.3mV/A

R_AC_LL : 10.3mV/A



Thermal protection

Need fine tune
 for thermal protect point
 Note placement position
 TEMP=85C

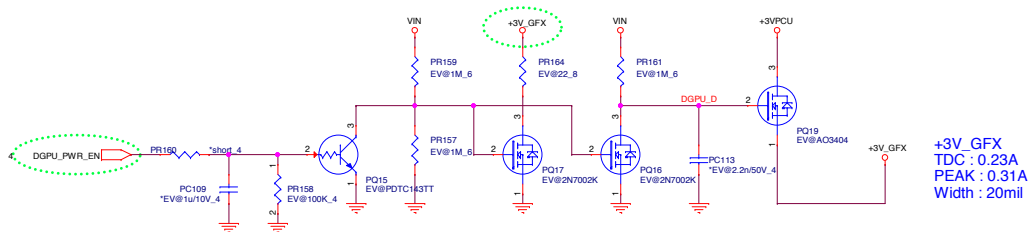
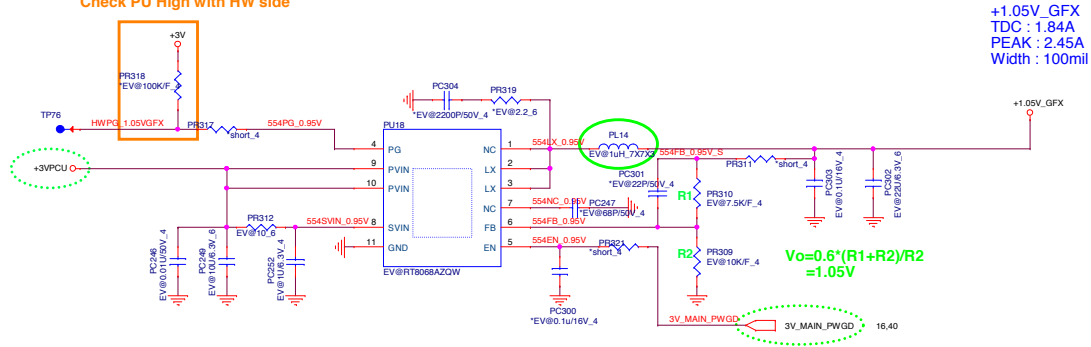


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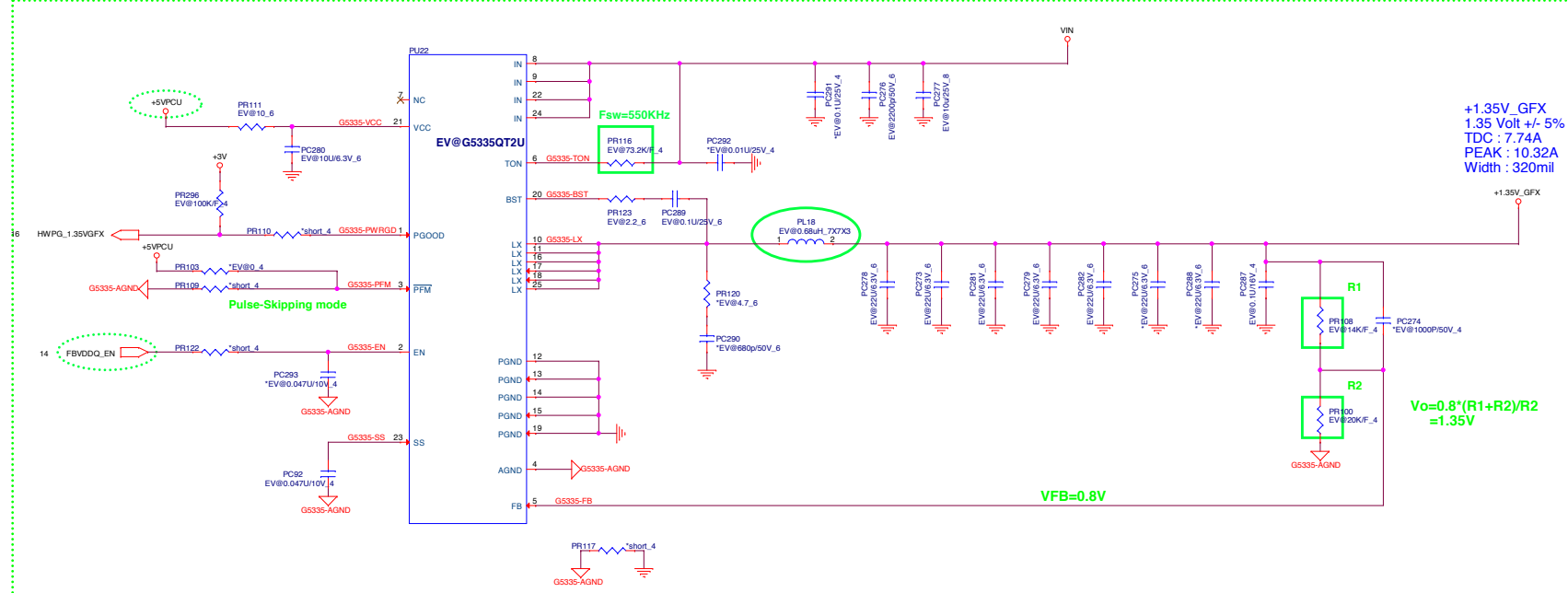
Size	Document Number	Rev
	+1.8V/+1.5V/Thermal Protect	1A
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14,15,16
+1.05V_GFX
14,16,17,30
+3V_GFX
15,19
+1.35V_GFX

Check PU High with HW side



+1.35V_GFX for GDDR5

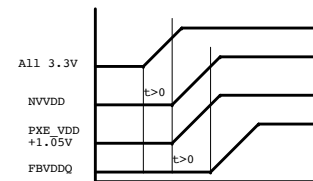
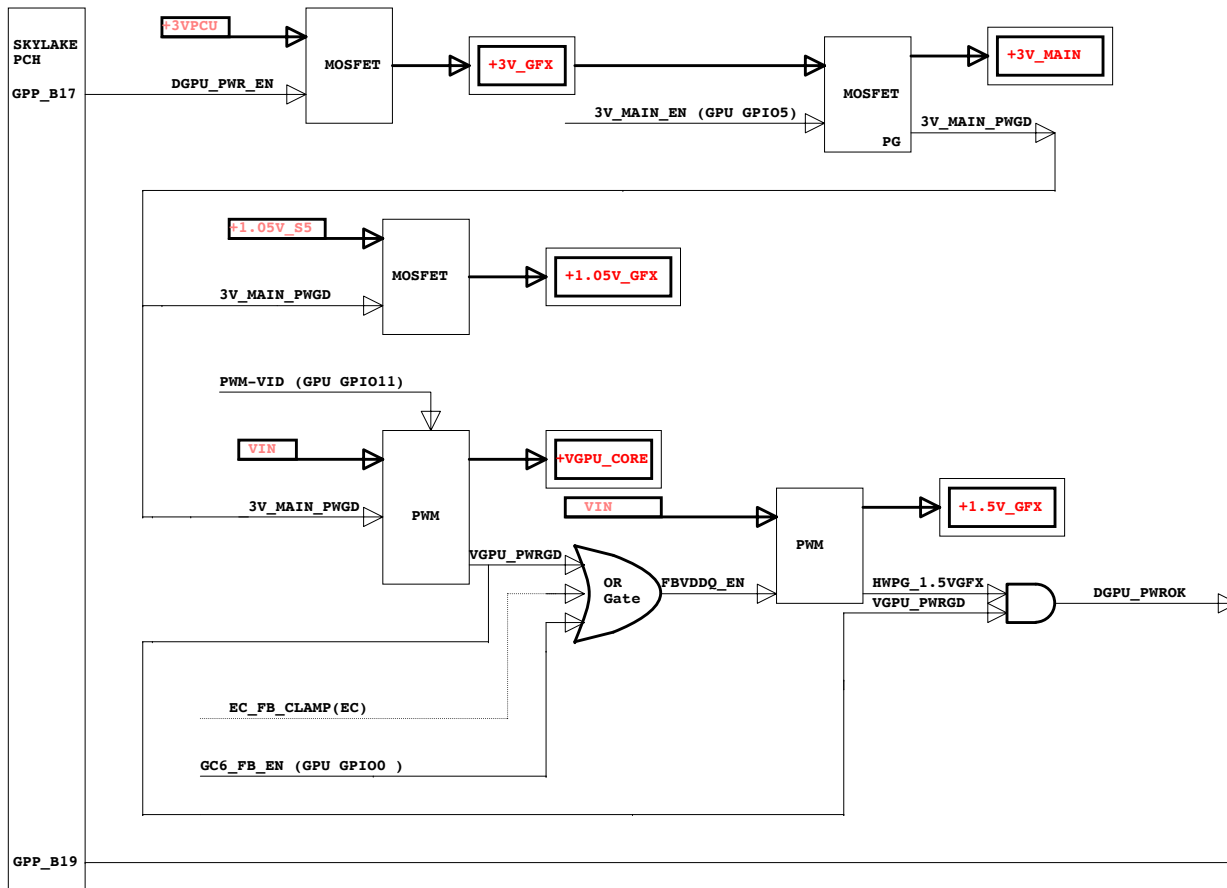


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PROJECT : ZAA

Size Document Number
+1.35V_GFX/+1.05V_GFX/+3V_GFX
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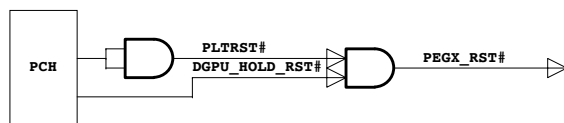
Rev
1A

VGA power up sequence

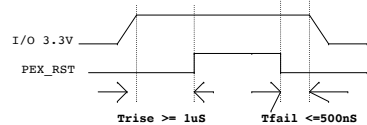


N15x Power on sequence
 Notes: -All 3.3V includes all rails powered at 3.3V
 -PEX_VDD 1.05V includes all rails that are shared

VGA Reset

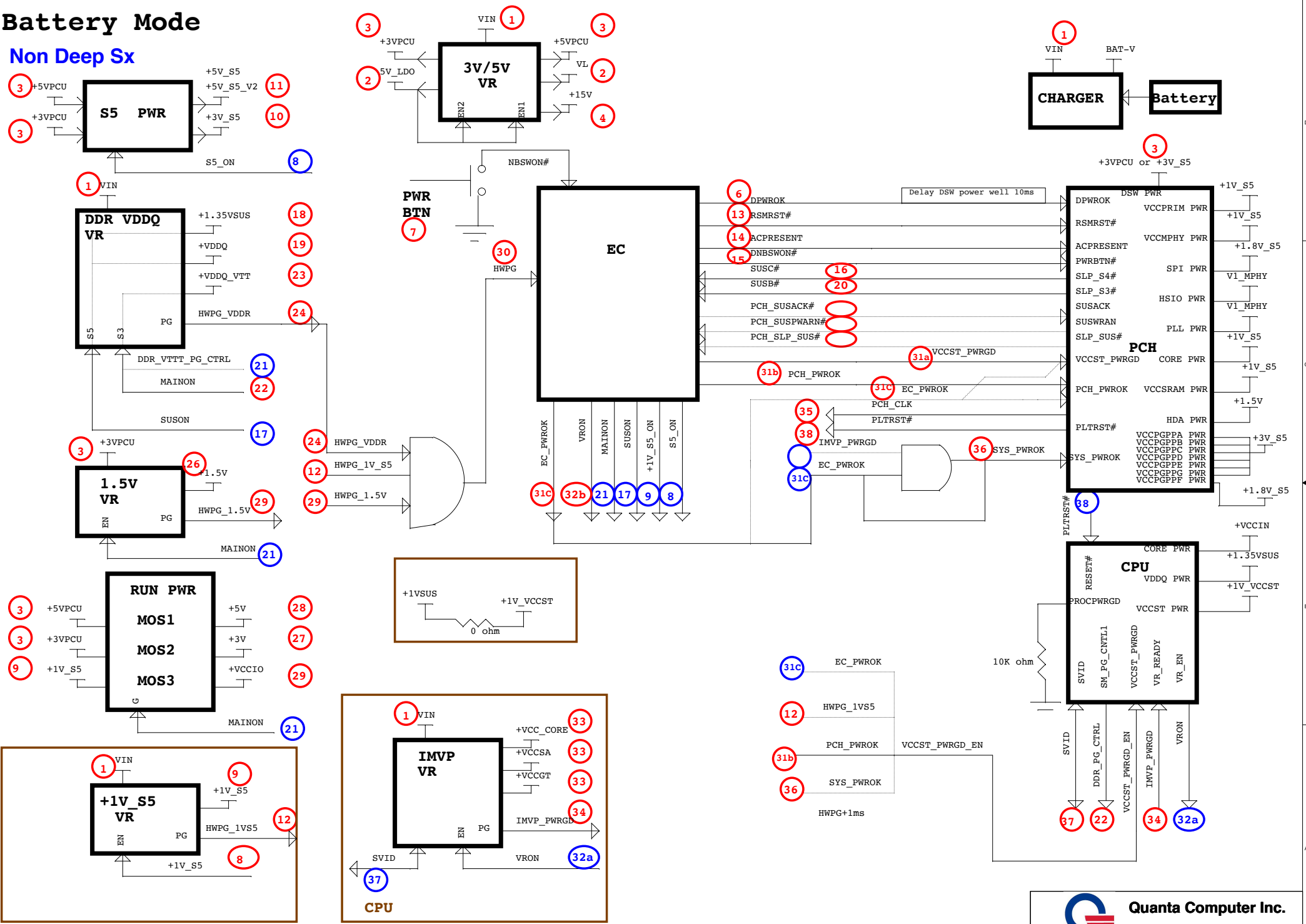


PEX_RST timing

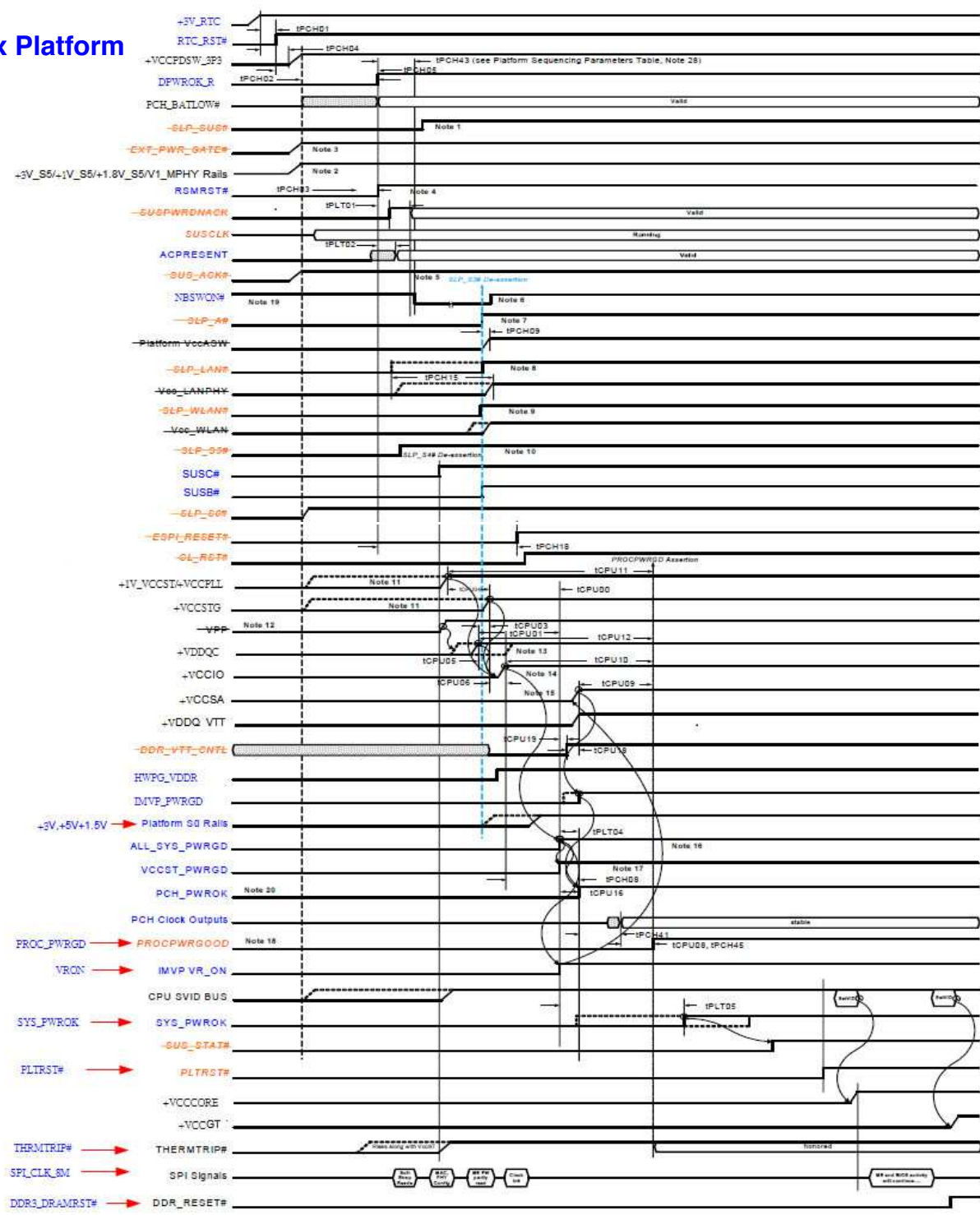


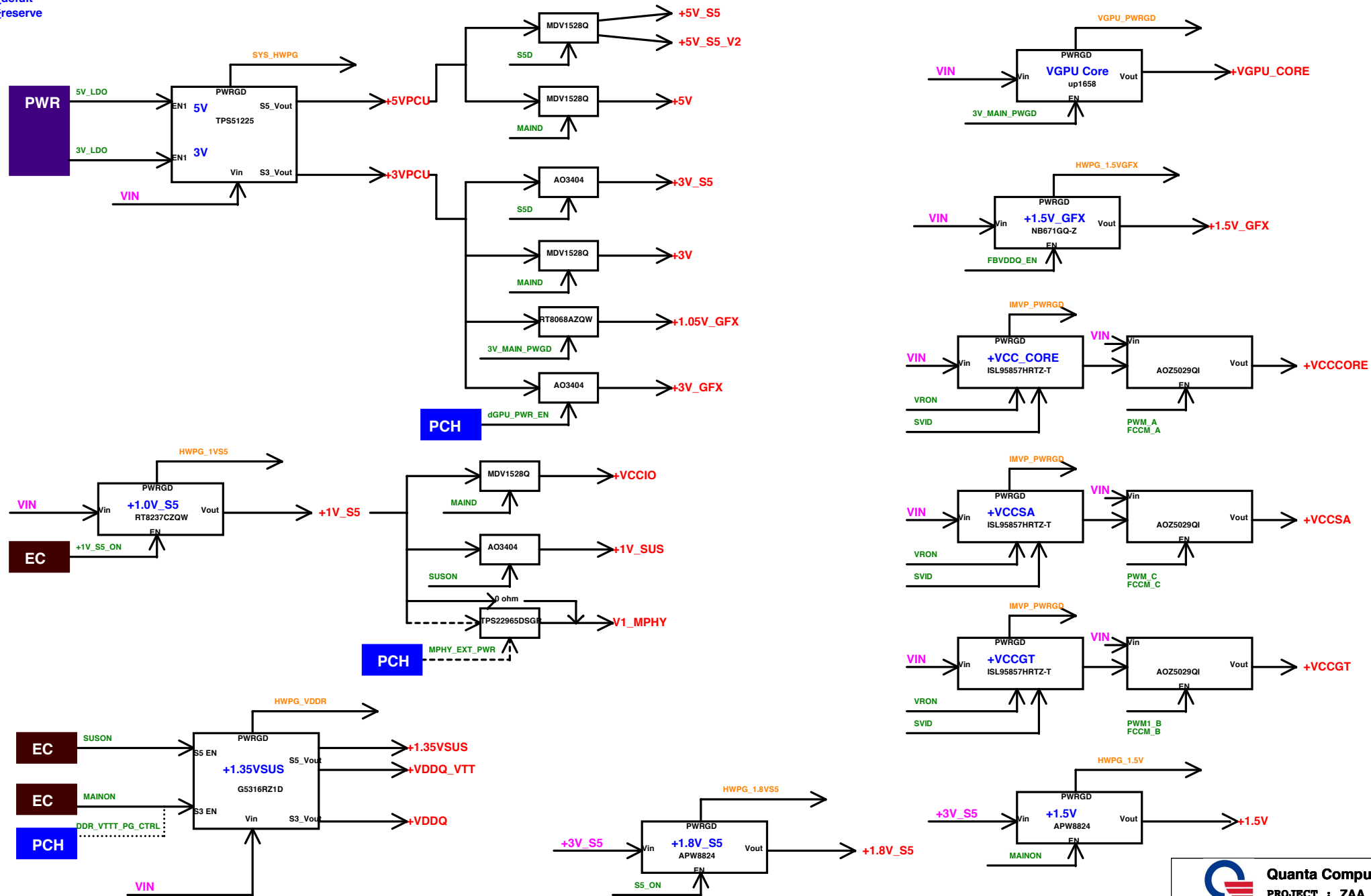
Battery Mode

Non Deep Sx

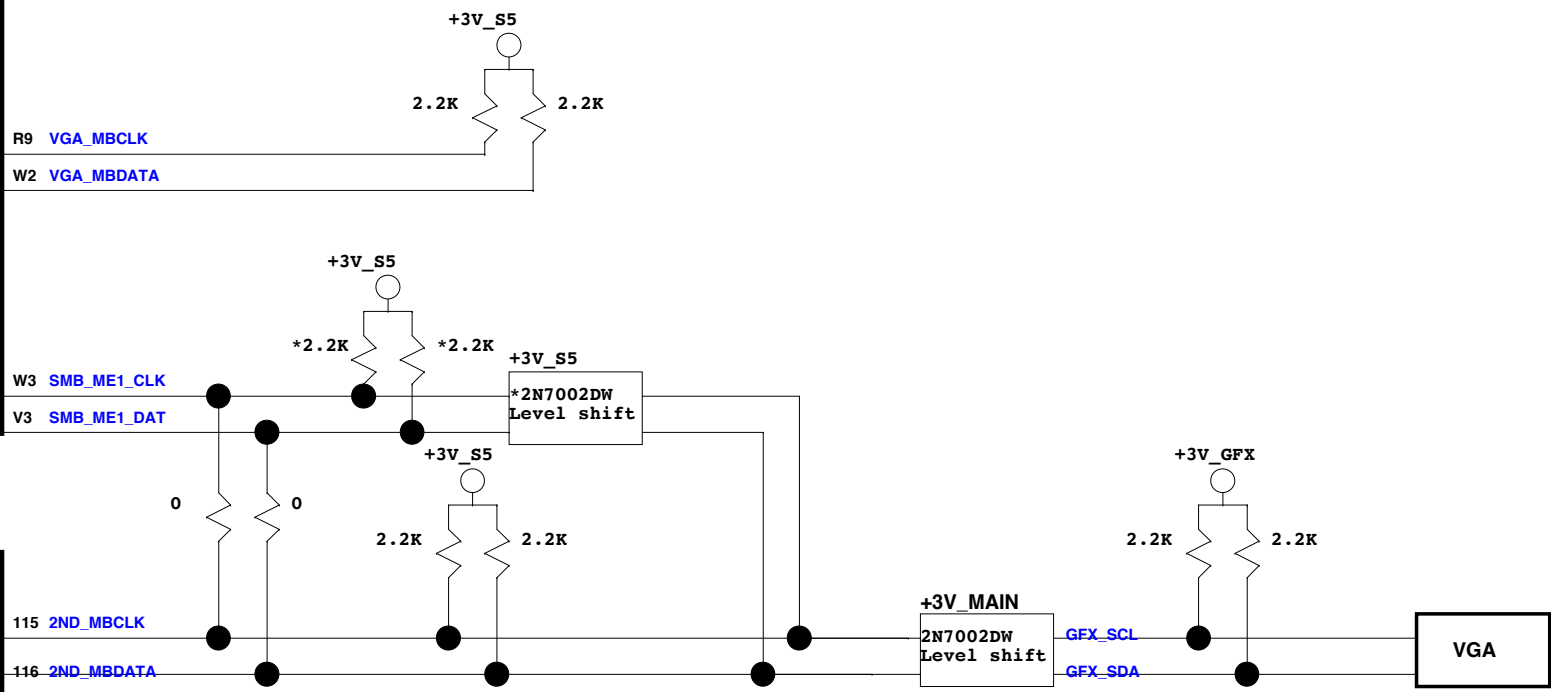
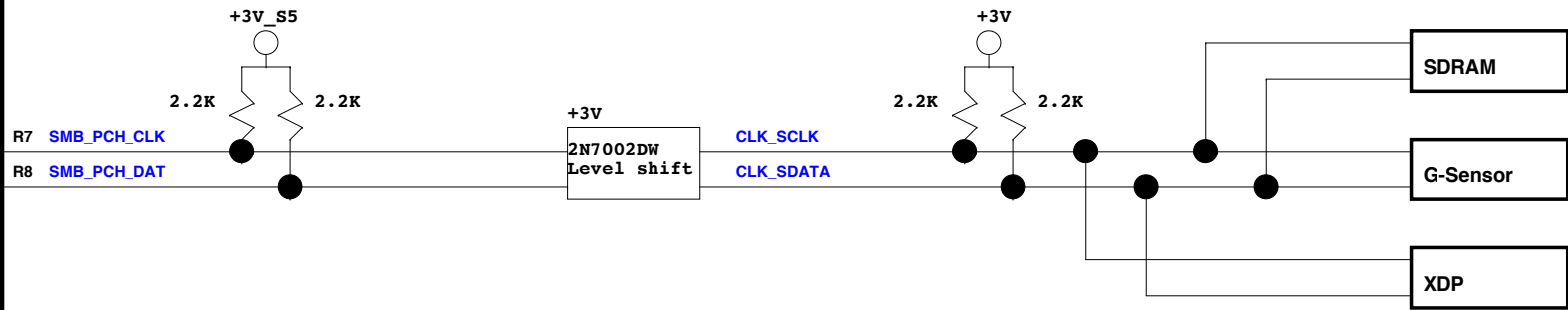


Skylake U Non-Deep Sx Platform
Power on sequence

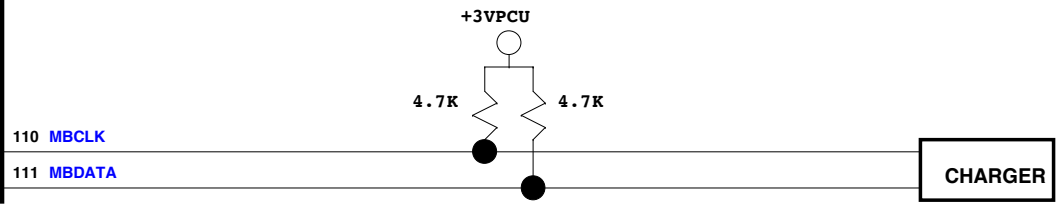





Skylake U



EC
IT8987CX



Stage	Date	CHANGE LIST
A	11/25	1. FIRST RELEASED
B	12/11	1. Update DFDS15FR421, DFFC28FR026, DFFC08FR055, DFFC04FR127 to new footprint. 2. Remove IOAC8 part and change BOARD_ID3 to low (page 8.) 3. Change FAN connector CN8 to 3-pin, and add releven circuits. (page 28.) 4. For FAN function change, swap U45 pin-81 with pin-32. (page 30.) 5. Reserve G-sensor circuit. (page 28.) 6. Internal speaker signal short pad R419, R414, R406 & R404 change to 0603 0 ohm. (page 25.) 7. Remove extra hall-sensor circuit on 17". (page 22.) 8. Modify touchpad INT circuit by using R164. (page 4.) 9. Add EC52 TVS diode. (page 30.) 10. Dual DMIC LR pin change to pull-high. (page 25.) 11. Change R4314 & R4306 of value for KA/KB (page 17.) 12. Change R247 value from 0 to 2.2 Ohm (CS-2204FA00). (page 24.) 13. Change R251, R262, R269, R11265 footprint from 0603 to 0805 (page 24.) 14. Reserve R11282 for battery. (page 30.) 15. Change CN23 H=5.0 part number (page 28.) 16. R512 Change to 1% tolerance part number (page 6.)
	12/14	1. Update CN6, CN8, CN18 part nmuber and foot print (page 25.) 2. Change U1006 part number to AL000103006 (page 26.) 3. Q6060 change to stuff (page 6.) 4. R628, R512, R630, R651, R4006 Change to 1% tolerance part number.
	12/15	1. Update HOLE1, HOLE2 foot print to new Rev (page 27.) 2. Add HOLE25, PAD14 foot print (page 27.) 3. Change CN13, CN16 foot print to new Rev (page 23.) 4. Change cap CP to normal cap for keyboard (page 22.) 5. Reserve POA(FPD) circuit (page 26.)
	12/20	1. Change PJ3 foot print to 50320-0040n-001-4p-1-smt for SMT issue (page 31.) 2. Change CPU 0201 Cap to 0402 besides C245, C196, C269, C285, C235 (page 5.) 3. Change SW4 foot print and part number for B-stage, and swap the pin (page 30.) 4. Modify some SPAD and HOLE (page 27.) 5. Change CN6 foot print to 50591-00401-001-4p-1 (page 28.) 6. Modify U22 Block GND pin 18-22 (page 29.) 7. Modify CN12, JDIM1, JDIM2, CN23, SW1, SW2 foot print to newer.
	12/21	1. Change CN2021 foot print to ub31-dx07b024xjlar1000-24p (page 20.) 2. Change CN10 foot print to ngff-nase0-s6701-ts48-ke-smt (page 27.) 3. Add R11284 reserve DMIC power supply (page 25.) 4. Change C739 to 22pF and stuff for bit clock issue (page 4.)
	12/22	1. Change C1255, C1257, C1265, C1270, C1327, C4728 to 10uF cap for cost down (page 12, page 13.)
	12/23	1. Modify R211, R152 to +3V_S5 for +3V leakage issue (page 8, page2.) 2. Modify R577 to reserved (NC), because no used (page 2.) 3. Add C4817, C4818, C4819, C4820 for EMI issue (page 20.) 4. Change CN2021 foot print to ub31-dx07b024xjlar1000-24p-smt (page 20.) 5. Change CN13, C16 foot print to ub3-yusb0021-p001a-9p-smt (page 29.) 6. Stuff R786, R568, R570, and unstuff U33, C628 (page 2, page 6.) 7. Swap PJ3 (page 31.)
	12/24	1. Change CN4 foot print to sdcard-psdat4-11glbslnn4h4-11p (page 24.) 2. Change R11267, R11270 to short pad, and change R11268, R11271 form 33 ohm to 47 ohm (page 22.) 3. Unstuff C319, C333, C336, C716, C718 (page 22.) 4. Reserve R11285, R11286 pull up to +3V, and R11287 pull down to GND for CRT issue (page 21.) 5. Stuff R11286 for CRT issue (page 21.) 6. Remove all type-C re-driver short resistor and capacitor (page 20.)
	12/25	1. Change HOLE16 foot print to H-TC217BC197D126P2 (page 24.)
	12/29	1. Modify the power solution between GT2 and GT3e, see the table (page 36.) 2. Change the power value, PC10 to 1uF CH5101K9B01 (page 36.) 3. Change the power value, PC20 to 0.022uF CH3224K1B01 (page 36.) 4. Change the power value, PC28 to 560pF CH1566K1B09 (page 36.) 5. Change the power value, PC39 to 0.015uF CH3154K1B00 (page 36.) 6. Change the power value, PR220 to 475 ohm CS14752FB11 (page 36.) 7. Modify BOARD_ID7. GPU GT, KB, GTR PU 10k ohm, KA PD 10k. (page 8.) 8. Change the RTC clock crystal Y2 part number to BG3327680C6 (page 6.) 9. Change Q115, Q129 part number to BAM70020076 (page 19.) 10. Modify R11283 to +3V fixed the SSD issue (page 27.) 11. Change the HOLE16 NUT part number to MBZAA002010 (page 27.)
	1/7	1. Remove R11274 and mount R11277 for change equalizer setting from 6dB to 4dB (page. 23) 2. Change 15" and 17" keyboard part number to DFFC28FR030 (page 28.)
B2	1/18	1. Update the System Block Diagram (page 1.) 2. Update the part number option same as B-SMT BOM.
	1/19	1. Power team remove JUMP and change 0 ohm to shortpad (page 31-41.) 2. Modify some description, value and part number have blank.
	1/20	1. Change C144,C150,C190,C199,C248,C645,C650,C659,C666,C690,C696,C697,C702 to 22uF, part number : CH6221M9A00 (page 5.) 2. Change C171,C178,C203,C219,C224,C226,C233,C236,C243,C251,C255,C272,C273,C282,C289,C691,C692,C693,C694,C703,C704,C705,C706,C707,C202,C210 to 10uF, part number : CH6101M9905 (page 5.)
	1/21	1. Change D2,D3,D4,D5,D4013,D4014,EC51,EC52 main source part number from BC040201Z00 to BC005725Z00.

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Date		Revision		Sheet									
March 28, 2016		1		1 of 1									

Stage	Date	CHANGE LIST
C	1/22	1. Reserve R11288, R11289, R11290, R11291 0ohm for POA NC function (page 26.) 2. Change Q115, Q129 main source to BAM70020002 3. Change Q5, Q4201 main source to BA039040020. 4. Change D7, D4000 main source to BCBAT54CZ01. 5. Change Q3, Q32, Q4301 main source to BAM70020047.
	1/26	1. Change CN5 part number to DFHS40FS036 (page 22.) 2. Change CN4 part number to DFHS11FR170 (page 4.) 3. Modify POA circuit for C-stage test (page 26.)
	1/27	1. Change the TPS25810RVC pu-high power from +5V_S5_V2 to +3V_S5 (page 20.) 2. Reserve R11193 for Type-C detec issue (page 20.) 3. Change 0 Ohm to short pad R11,R14,R15,R28,R66,R67,R11129,R102,R194,R224,R229,R235,R790,R791,R792,R11111,R11112,R11113,R11140,R112,R135,R179,R180,R182,R185,R187,R188,R192,R193,R198,R240,R252,R11131,R164,R246,R339,R350,R11185,R11186,R550,R657,R718,R721,R782,R11153,R11283,R795,R796,R797,R816,R817,R818,R819,R820,R821,R11196,R11199,R11202,R11207,R11279,R11280,R11281,R948,R951,R956,R958,R959,R960,R11061,R11062,R11110,R11133,R11134,R11136,R11137,R11138,R11139,R11141,R11253,R11254,R11255,R11256,R11267,R11270,R4328,R4335,R2855,R2870,R318,R221,R403,R405,R742,R743,R725,R745,L19,R2872. 4. Add TYPE8 part at Type-C power function (page 32.) 5. Add BL8 part at keyboard back-light (page 28.) 6. Reserve 15" 17" Dual DMIC circuit part (page 25.) 7. Reserve C4821 for NAC function (page 24.)
	1/28	1. Add EV8 part at HOLE8, HOLE9 (page 27.)
	1/29	1. Stuff PR233, PR234 for GT3e power function (page 37.) 2. Add D228, D108 part at CPU power side (page 5.) 3. Change PR209, PR210 from short pad to 10 ohm (page 31.)
	2/2	1. Modify POA circuit for C-stage test (page 26.) 2. Remove HOLE25 because not used (page 25.) 3. Change HOLE13, HOLE14, HOLE15 foot print to H-C256D161P2 (page 25.)
	2/3	1. Modify POA circuit for C-stage test (page 26.) 2. Change PC115 from CH5104K9906 to CH41006K911 for FAE suggest (page31.) 3. Stuff PC138 for FAE suggest (page 37.)
	2/4	1. Update C-test BOM.
	2/16	1. Change PR6121 from CS31002FB26 to CS29312FB13 (page 32.) 2. Add C376 distinguish ZAA/ZAAA 15" serial and ZYJ/ZYI 17" serial (page 25.) 3. Change LED current limiting resistor blue and orange to 47 ohm and 124 ohm (page 28.)
	2/17	1. Change PU6010 from AL006575002 to AL051225003 for 3/5V IC noise issue (page 32.)
RAMP	2/22	1. Stuff PC6229, PC6212 for 3/5 voltage IC noise and charging issue (page 32, 37.) 2. Change PR183, PR184, PR209, PR210 to shortpad for 3/5 voltage IC noise and charging issue (page 31.) 3. Modify RP1 circuit (page 28.)
	3/3	1. Unstuff R694, R699 (page 27.) 2. Change 0 Ohm to shortpad R3, R4 R365, R640, R653, R659, R668, R11191, R11192, R16, R212, R404, R406, R414, R419, R752, R789, R237, R672. 3. Remove RP2, RP3, RP4, RP5, L69 for SMT colay issue. (page 20.)
	3/9	1. Change 0 Ohm to shortpad R11284, R2870, R2872, R11298, PR6296, R4329, R4336, PR112. 2. Change PR201, PR202 and PR211 to 1.5k, 97.6k and 267 ohm for GT2 and GT3 (page 36.) 3. Add PC6232, PC6233 at 3/5 V Vin (page 32.) 4. Change PL6013 from 1uH_7X7X3 to 2.2uH_7X7X3 (page 32.)
	3/10	1. Change C714 and C724 value from 10p to 1000p for projector issue (page 22.) 2. Remove SW2 for RAMP-stage (page 30.) 3. Change PU10, PU11, PU20 footprint to son14-3x2-4-15p-smt (page 32.)
	3/15	1. Change RTC crystal circuit C351 and C362 value from 6.8p to 15p for EA issue (page 22.) 2. Modify GPU power solution for cost down (page 40.)
	3/25	1. Change R237 shortpad to 0 ohm for next PCB rev. F (page 27.) 2. Reserve POA function (page 26.)

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